Patentability Search Report
MVB Communication Module
(Docket No: LEX077P002)

Prepared By:

On the request of:

Date: July 16, 2025

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1. Key inventive concept

The proposed invention relates to…

2. Search Focus

Both patents & non-patent literature disclosing the below concepts were considered. The shortlisted documents are provided with respective relevant excerpts:

1. A

   1.1.

3. Search Methodology

Step 1: Understanding and Making Search Strategy

- An in-depth understanding of the "**MVB Communication Module**" was analyzed in terms of project requirements.
- A thorough study of the technology domain was performed by web research to gather relevant information.
- Key concepts are identified and defined using keywords and their synonyms.
- Key strings are prepared based on identified search terms, and relevant patent classifications.

Step 2: Searching and Analysis

- A broad-to-narrow search strategy (or narrow-to-broad) was employed using various search strings on a few commercial/free databases to identify patents/applications.
- The extracted documents are analyzed in detail to identify potentially relevant documents which were further segregated as relevant and related depending on number of features matching with the technical features of the study.
- For Patent literature only one member per family is considered for analysis.
- For non-English documents, the analysis is carried out based on machine-translated text available from free/commercial sources.

Step 3: Additional Searches

To ensure search comprehensiveness, the following searches were performed**:**

- Inventor/Assignee based search - The assignee/inventor of client's interest or the assignee/inventor from the identified shortlisted documents.
- IPC/CPC/ECLA/US search - Various classes are used with/without the combination of keywords.
- Semantic - Commercial databases are used to search on contextual meaning of terms.
- Similarity search - A similarity search of the target patent and identified relevant prior art is conducted in the commercial databases
- Citation Search - Two level citation searches of closely identified prior arts are executed.

Step 4: Report

- The shortlisted relevant documents along with the bibliographic details and text mapping are provided in a user-friendly, MS Word/PDF report.
- Related documents are provided in the form of list in the report.
- Bibliographic details of both relevant and related documents are provided in the report.
- All the documents are provided with hyperlinks to respective patent office sites or Espacenet.
- A tabulated summary of the relevant references is provided with executive summary.

4. Database Used

Patent Databases	Non-Patent Databases
✓ Questel Orbit ✓ Dolcera Patent Categorization System ✓ Google Patents ✓ Espacenet ✓ USPTO ✓ Free Patents Online	✓ General Google search ✓ Google Scholar ✓ Science Direct ✓ IEEE ✓ Springer, etc.

5. Relevant Keywords

Key words	Synonyms/Alternative terms
Multifunction vehicle bus	MVB, fieldbus, train bus, network, interface, data bus
Field programmable gate array	FPGA, chip, logic, controller, processor, reconfigurable, programmable, chip, controller, software-defined hardware
Enclosure	metallic housing, casing, case, box, shell, cabinet, cover, container, cage
Railway	train, rollingstock, coach, locomotive, transit, rail
Communication	signalling, messaging, data, networking, interface, exchange
Module	unit, board, device, block, component, subsystem
Interface	connector, port, link, bridge, junction, connection
Real-Time	instant, live, immediate, synchronous, direct, timely
Compact	small, mini, tight, dense, slim, concise
Rugged	durable, strong, tough, sturdy, shockproof, hard, harsh conditions, industrial-grade use, railway-grade
Protection	shielding, isolation, safety, defence, guard, prevention
Connector	plug, interface, jack, port, terminal, pin
Redundancy	backup, reserve, safety, duplicate, spare, fault-tolerant
IEC 61375	railway communication standard, train communication protocol
Protocol Interfacing	bus interface, data link interface, communication stack integration
Electrical Interfacing	signal conditioning, voltage level adaptation, i/o matching
Mechanical Ruggedness	shock resistance, vibration tolerance, mechanical reliability, harsh reality

6. Classification Codes

IPC/CPC Codes	Definition
B	Performing operations; transporting
B61	Railways
B61L	Guiding railway traffic; ensuring the safety of railway traffic
B61L15/00	Indicators provided on the vehicle or train for signalling purposes
B61L15/0027	Radio-based, e.g. Using gsm-r
B61L15/0036	Conductor-based, e.g. Using can-bus, train-line or optical fibres
G	Physics
G01	Measuring; testing
G01R	Measuring electric variables; measuring magnetic variables
G01R31/00	Arrangements for testing electric properties; arrangements for locating electric faults; arrangements for electrical testing characterised by what is being tested not provided for elsewhere
G05	Controlling; regulating
G05B	Control or regulating systems in general; functional elements of such systems; monitoring or testing arrangements for such systems or elements
G05B23/00	Testing or monitoring of control systems or parts thereof
G05B23/02	Electric testing or monitoring
G05B23/0205	Electric testing or monitoring by means of a monitoring system capable of detecting and responding to faults
G05B23/0208	Electric testing or monitoring by means of a monitoring system capable of detecting and responding to faults characterised by the configuration of the monitoring system
G05B23/0213	Modular or universal configuration of the monitoring system, e.g. Monitoring system having modules that may be combined to build monitoring program; monitoring system that can be applied to legacy systems; adaptable monitoring system; using different communication protocols
G06	Computing; calculating or counting
G06F	Electric digital data processing
G06F13/00	Interconnection of, or transfer of information or other signals between, memories, input/output devices or central processing units
G06F13/40	Bus structure
G08	Signalling
G08B	Signalling or calling systems; order telegraphs; alarm systems
G08B17/00	Fire alarms; alarms responsive to explosion
H	Electricity
H04	Electric communication technique
H04L	Transmission of digital information, e.g., telegraphic communication
H04L12/00	Data switching networks

H04L12/28	Data switching networks are characterised by path configuration, e.g. Lan [local area networks] or wan [wide area networks]
H04L12/40	Bus networks
H04L12/40006	Architecture of a communication node
H04L12/40052	High-speed ieee 1394 serial bus
H04L12/40097	Interconnection with other networks
H04L12/4013	Management of data rate on the bus
H04L12/40143	Bus networks involving priority mechanisms
H04L12/40169	Flexible bus arrangements
H04L12/40176	Flexible bus arrangements involving redundancy
H04L2012/40215	Controller area network can
H04L12/403	Bus networks with centralised control, e.g. Polling
H04L12/407	Bus networks with decentralised control
H04L12/66	Arrangements for connecting between networks having differing types of switching systems, e.g. Gateways
H04L41/00	Arrangements for maintenance, administration or management of data switching networks, e.g. Of packet switching networks
H04L41/06	Management of faults, events, alarms or notifications
H04L41/0654	Management of faults, events, alarms or notifications using network fault recovery
H04L67/00	Network arrangements or protocols for supporting network services or applications
H04L67/2866	Architectures; arrangements
H04L2012/40208	Bus networks characterised by the use of a particular bus standard
H04L2012/4026	Bus for use in automation systems
H04L2012/40267	Bus for use in transportation systems
H04W	Wireless communication networks
H04W4/00	Services specially adapted for wireless communication networks; facilities therefor
H04W4/30	Services specially adapted for particular environments, situations or purposes
H04W4/40	Services specially adapted for particular environments, situations or purposes for vehicles, e.g. Vehicle-to-pedestrians [v2p]
H04W4/44	Services specially adapted for particular environments, situations or purposes for vehicles, e.g. Vehicle-to-pedestrians [v2p] for communication between vehicles and infrastructures, e.g. Vehicle-to-cloud [v2c] or vehicle-to-home [v2h]
H04W24/02	Arrangements for optimising operational condition

7. Search and Analysis Summary

Feature No.	REFERENCES (Category***)					
	CN105429837A (Y)	CN112684780A (Y)	CN104361652A (Y)	CN220190895U (Y)	CN209514377U (Y)	US9565270B2 (Y)
1.	✓	✓*	✓	✓*	✓*	✓*
1.1.	✓	✓	✓	✓	✓	✓
1.1.1.	✓	✓	✓	✓	✓	✓
1.1.2.	✓	✓*	✓*	✓*	✓*	-
1.1.3.	✓*	✓*	✓*	✓*	-	-
1.1.4.	✓*	✓	✓*	✓	✓	✓*
1.1.5.	✓*	✓*	✓	-	-	-
1.1.6.	✓*	✓	✓*	✓*	-	-
1.1.7.	✓*	-	✓*	✓*	✓*	-
1.2.	✓	✓	-	✓*	✓*	-
1.3.	✓*	✓*	✓*	-	✓*	✓
1.4.	✓*	✓	✓*	✓	✓*	✓

***Reference Category

X- Possibly relevant taken alone
Y- Possibly relevant combined with another Y document
D- Cited in the invention disclosure
A- General state of art/background technology

✓- Fully mapped
✓*- Partially mapped

*Please note that the relevancy ranking above is based on LexAnalytico analyst/non-patent attorney's opinion, and it may significantly change depending on many circumstances.

8. Relevant References: Patent Literature

Back to Analysis Summary

Publication No.	**CN105429837A**		
Title	MVB repeater		
Assignee/Applicant	China Academy of Railway Sciences Corp. Ltd.		
Earliest Priority Date	2015-12-25	**Publication Date**	2016-03-23

Abstract

The invention provides an MVB repeater. The MVB repeater comprises a shell and a circuit board card fixed in the shell; the circuit board card comprises two channel circuits, which are redundant with each other and independent; each channel circuit comprises a first MVB signal driving and receiving circuit, a second MVB signal driving and receiving circuit, a power supply conversion module and an FPGA module; the first MVB signal driving and receiving circuit, the second MVB signal driving and receiving circuit and the FPGA module are respectively connected to the power supply conversion module; one end of the first MVB signal driving and receiving circuit is connected with a first segment MVB; the other end of the first MVB signal driving and receiving circuit is connected with one end of the FPGA module; one end of the second MVB signal driving and receiving circuit is connected with the other end of the FPGA module; the other end of the second MVB signal driving and receiving circuit is connected with a second segment MVB; the FPGA module receives an MVB signal from one of the first segment MVB and the second segment MVB; and, after being conditioned, the MVB signal is forwarded to the other one of the first segment MVB and the second segment MVB. The MVB repeater disclosed by the invention has high reliability.

Description

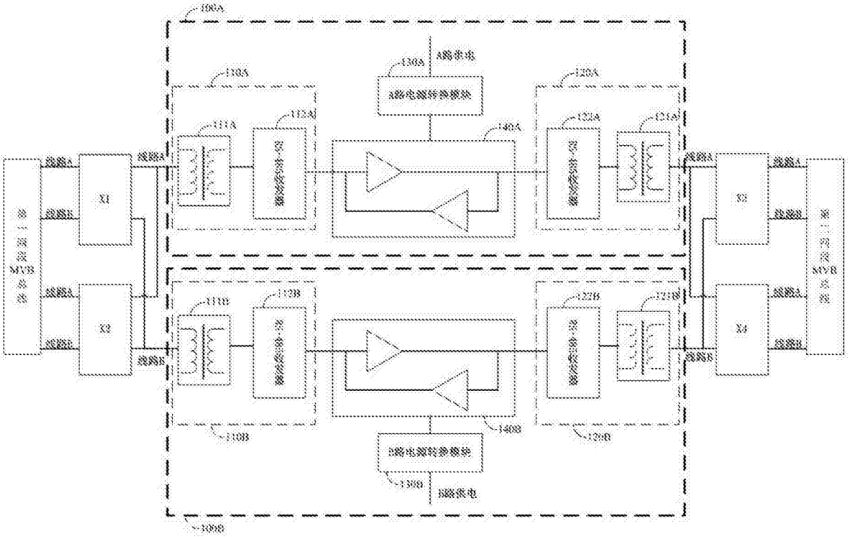
[Pages 17-18]

For the MVB repeaters of the above-mentioned embodiments, the circuit board cards thereof can be fixed in a housing. The shell has a certain strength and is used to encapsulate and fix the circuit board card, and can meet the vibration and impact requirements specified by railway standards. The shell can be in various shapes, such as a cubic shape, depending on specific needs.

[Pages 18-19]

The MVB repeater of the present invention can meet the test indicators and requirements for the MVB repeater in IEC61375-2. Moreover, the consistency test results of the developed MVB repeater show that it fully meets the requirements of

	the standard. The MVB repeaters of the present invention are respectively subjected to consistency tests of products of well-known foreign manufacturers, such as Siemens' MVB repeaters and Duagon's MVB repeaters, to achieve the interconnection and interoperability of MVB communications. The equipment is also certified to carry out electromagnetic compatibility tests, high and low temperature humidity tests, and vibration and shock tests for various railway standards. The MVB repeater of the present invention, as a communication device working in the physical layer of the MVB network, has the following characteristics.
	Description **[Page 18]** **For the MVB repeaters of the above-mentioned embodiments, the circuit board cards thereof can be fixed in a housing. The shell has a certain strength and is used to encapsulate and fix the circuit board card, and can meet the vibration and impact requirements specified by railway standards. The shell can be in various shapes, such as a cubic shape, depending on specific needs.**
	Description **[Page 3]** In one embodiment, **the FPGA module includes: a first receiving module, a second receiving module, a first sending module, a second sending module and a direction identification module; the direction identification module is connected between the first MVB signal driving receiving circuit and the second MVB signal driving receiving circuit to identify the transmission direction of the MVB signal between the first network segment MVB bus and the second network segment MVB bus; the first receiving module is used to receive the MVB signal from the first network segment MVB bus through the first MVB signal driving receiving circuit**; the first sending module is used to send the MVB signal from the first network segment MVB bus to the second MVB signal driving receiving circuit; the second receiving module is used to receive the MVB signal from the second network segment MVB bus through the second MVB signal driving receiving circuit; the second sending module is used to send the MVB signal from the second network segment MVB bus to the first MVB signal driving receiving circuit; wherein, when the direction identification module identifies that the transmission direction is from the first network segment MVB bus to the second network segment MVB bus, a sending enable signal is generated and sent to the second MVB signal driving receiving circuit; when the direction identification module identifies that the transmission direction is from the first network segment MVB bus to the second

	network segment MVB bus When the transmission direction is from the second network segment MVB bus to the first network segment MVB bus, a transmission enable signal is generated and sent to the first MVB signal driving receiving circuit.
	Description **[Page 4]** In one embodiment, the repeater further includes: **one or more of a power input protection circuit, a power filter circuit and an EMC suppression circuit arranged at the input end of the power conversion module.** **[Page 11]** In the embodiment of the present invention, before the input end of the power module, devices such as TVS diodes, varistors, conjugate coils, safety capacitors, etc. are used to design circuits such as power input protection, power filter circuits, and **EMC suppression circuits, which not only enable the MVB bus repeater to meet the EMC standards, but also realize protection and/or filtering of the power input.** **[Page 10]** As shown in FIG. 1 , **the first MVB signal driving receiving circuit 110A may include: a first isolation transformer 111A and a first RS-485 transceiver 112A connected to each other. The first RS-485 transceiver 112A is connected to the FPGA module 140A.**  图 1

	Description **[Page 4]** In one embodiment, the repeater further includes: **one or more of a power input protection circuit, a power filter circuit and an EMC suppression circuit arranged at the input end of the power conversion module.** **[Page 9]** In the embodiment of the present invention, **the power conversion module** does not adopt the method of connecting separate devices in the prior art, but adopts a mature and reliable switching power supply module, **which can fully meet the reliability indicators, electromagnetic compatibility indicators, power consumption, efficiency and other indicators of the repeater and the actual needs of the MVB repeater, and has high reliability.** **[Page 11]** In the embodiment of the present invention, **an RS-485 transceiver chip is selected as the physical layer chip, and its driving capability, receiving capability and anti-interference ability all meet the requirements of RS-485 and IEC61375 standards.** Moreover, the technology used by the RS-485 transceiver chip can keep the output level at a high level instead of a high impedance state when the bus is idle, which is beneficial to the logic design of the FPGA module. In addition, in an embodiment of the present invention, an isolation transformer is provided in the MVB signal driving receiving circuit, which not only meets the requirements of the EMD medium, but also can electrically isolate the MVB bus and the transceiver. For example, the insulation withstand voltage between the source side and the secondary side of the isolation transformer can reach 3KV, with high safety performance. In the embodiment of the present invention, before the input end of the power module, devices such as TVS diodes, varistors, conjugate coils, safety capacitors, etc. are used to design circuits such as power input protection, power filter circuits, and **EMC suppression circuits, which not only enable the MVB bus repeater to meet the EMC standards, but also realize protection and/or filtering of the power input.**
	Description **[Page 4]**

	In one embodiment, the repeater further includes: **one or more of a power input protection circuit, a power filter circuit and an EMC suppression circuit arranged at the input end of the power conversion module.** **[Page 9]** In the embodiment of the present invention, the repeater has a completely independent and redundant dual-channel structure, **each channel includes an independent power conversion module, which can provide an independent power supply, thereby significantly improving the reliability of the repeater. The power conversion modules of different channels can be connected to their respective power supplies using sockets, with dual redundant power supply and easy connection.** **The power conversion module 130A and the power conversion module 130B in the above hardware circuit board card can be two sets of completely independent and identical power conversion modules. The power conversion module (130A, 130B) can convert any DC power supply in the range of [43V, 160V] input from the outside into the DC power supply required by the FPGA module (140A, 140B) and the MVB signal driving receiving circuit (110A, 110B) (for example, RS-485 transceiver), such as a 5V DC power supply.** In the embodiment of the present invention, **the power conversion module** does not adopt the method of connecting separate devices in the prior art, but adopts a mature and reliable switching power supply module, **which can fully meet the reliability indicators, electromagnetic compatibility indicators, power consumption, efficiency and other indicators of the repeater and the actual needs of the MVB repeater, and has high reliability.**
	Description **[Page 4]** In one embodiment, the FPGA module also includes: a frame spacing **and edge jitter adjustment module, connected between the first receiving module and the first sending module, and between the second receiving module and the second sending module, for determining when the time spacing between the two frames of the MVB signal is less than a first set time value, delaying the next frame signal by a second set time value, and for determining when the jitter of the MVB signal is within a set time range, synchronizing the MVB signal according to a set clock.**

	[Page 16] **The frame spacing and edge jitter adjustment module 144 can be used to determine when the time interval between the two frame signals of the MVB signal is less than a first set time value,** for example, less than 4μs, and delay the latter frame signal by a second set time value, for example, a delay of 4μs. It can also be used to determine when the jitter of the MVB signal is within a set time range, for example, **the jitter is within a range of 125ns, and synchronize the input signal of the frame spacing and edge jitter adjustment module 144, for example, the MVB signal, according to a set clock.** Furthermore, if the jitter of the MVB signal exceeds the above-mentioned set time range (for example, the jitter exceeds the 125ns range), it can be processed as a collision and the MVB signal can be directly forwarded to the sending module (1421, 1422) to ultimately forward the MVB signal to the target network segment MVB bus.
	Description **[Page 5]** In one embodiment, the repeater further includes: **an output voltage protection circuit and /or an output voltage filtering circuit; the output voltage protection circuit and the output voltage filtering circuit are both arranged at the output end of the power conversion module.** **[Page 5]** In one embodiment, the repeater also includes: **a first bus end overvoltage protection circuit and/or a second bus end overvoltage protection circuit; wherein the first bus end overvoltage protection circuit is connected between the first network segment MVB bus and the first MVB signal driving receiving circuit;** the second bus end overvoltage protection circuit is connected between the second network segment MVB bus and the second MVB signal driving receiving circuit.
	Description **[Pages 17-18]** For the MVB repeaters of the above-mentioned embodiments**, the circuit board cards thereof can be fixed in a housing. The shell has a certain strength and is used to encapsulate and fix the circuit board card, and can meet the vibration and impact requirements specified by railway standards. The shell can be in various shapes, such as a cubic shape, depending on specific needs.** **[Pages 18-19]**

	The MVB repeater of the present invention can meet the test indicators and requirements for the MVB repeater in IEC61375-2. Moreover, the consistency test results of the developed MVB repeater show that it fully meets the requirements of the standard. **The MVB repeaters of the present invention are respectively subjected to consistency tests of products of well-known foreign manufacturers, such as Siemens' MVB repeaters and Duagon's MVB repeaters, to achieve the interconnection and interoperability of MVB communications. The equipment is also certified to carry out electromagnetic compatibility tests, high and low temperature humidity tests, and vibration and shock tests for various railway standards. The MVB repeater of the present invention, as a communication device working in the physical layer of the MVB network, has the following characteristics**
	Description **[Page 18]** **Preferably, the housing is made of metal to shield the external electromagnetic interference of the circuit board card and better adapt to the electromagnetic environment specified by the electromagnetic compatibility standard.** **Furthermore, preferably, the object is an integrally formed metal shell, which can be formed in one step using an integral mold. In this way, the sealing effect is good and the metal housing has a better ability to shield the external electromagnetic interference of the circuit board card.**
	Description **[Page 4]** In one embodiment, the FPGA module also includes: a frame spacing and edge jitter adjustment module, connected between the first receiving module and the first sending module, and between the second receiving module and the second sending module, **for determining when the time spacing between the two frames of the MVB signal is less than a first set time value, delaying the next frame signal by a second set time value, and for determining when the jitter of the MVB signal is within a set time range, synchronizing the MVB signal according to a set clock.** In one embodiment, **the FPGA module also includes: a bus idle and Jabber fault identification module, connected between the first MVB signal driving receiving circuit and the second MVB signal driving receiving circuit; when the bus idle and Jabber fault identification module determines that the continuous idle time of the**

	source network segment line identified by the direction identification module exceeds a third set time value, the bus idle and Jabber fault identification module controls the direction identification module to re-identify the transmission direction of the MVB signal, and when it is detected that the source network segment line continues to send the MVB signal for more than a fourth set time value, the first sending module or the second sending module stops sending the MVB signal to the target network segment line identified by the direction identification module until the continuous idle time of the target network segment line exceeds a fifth set time value. **[Page 15]** In a preferred embodiment, the first receiving module 1411 and the second receiving module 1412 can determine whether the MVB signal is a normal frame signal or a collision frame signal by sampling the MVB signal, and can perform waveform conditioning and signal shaping on the normal frame signal according to the IEC61375 standard through, for example, **the frame spacing and edge jitter adjustment module in the FPGA module, and directly forward the collision signal without performing timing adjustment. For example, if the receiving module (1411, 1412) detects that the MVB signal is a normal frame signal, it can be directly sent to the subsequent modules, such as the sending module (1421, 1422). If the MVB signal is detected to be a collision frame signal, the FPGA module directly starts sending and forwards the source signal. In this way, the reliability of the MVB repeater can be improved.**
	Description **Page 4]** In one embodiment, the FPGA module also includes: a frame spacing and edge jitter adjustment module, connected between the first receiving module and the first sending module, and between the second receiving module and the second sending module, **for determining when the time spacing between the two frames of the MVB signal is less than a first set time value, delaying the next frame signal by a second set time value, and for determining when the jitter of the MVB signal is within a set time range, synchronizing the MVB signal according to a set clock.** In one embodiment, **the FPGA module also includes: a bus idle and Jabber fault identification module, connected between the first MVB signal driving receiving circuit and the second MVB signal driving receiving circuit; when the bus idle and Jabber fault identification module determines that the continuous idle time of the source network segment line identified by the direction identification module**

	exceeds a third set time value, the bus idle and Jabber fault identification module controls the direction identification module to re-identify the transmission direction of the MVB signal, and when it is detected that the source network segment line continues to send the MVB signal for more than a fourth set time value, the first sending module or the second sending module stops sending the MVB signal to the target network segment line identified by the direction identification module until the continuous idle time of the target network segment line exceeds a fifth set time value. **[Page 7]** **The present invention provides an MVB bus repeater, which has a dual-channel structure, each channel is provided with an independent power supply, and adopts a unique FPGA design, can achieve a variety of excellent technical characteristics, and can meet the test indicators and requirements for MVB repeaters in the IEC61375-2 international standard.** **[Page 10]** **The first RS-485 transceiver 112A and the second RS-485 transceiver 122A may both use RS485 driver chips, and may be used to implement the physical layer of the first MVB network segment and the physical layer of the second MVB network segment. In other words, the first RS-485 transceiver 112A can be used to receive the signal of MVB line A from the MVB bus of the first network segment, and convert the received MVB signal into a logic signal of, for example, 5V. At the same time, the RS-485 transceiver 112A drives the forwarding signal from the FPGA module 140A into an RS-485 signal and sends it to line A of the MVB bus of the first network segment;** the second RS-485 transceiver 122A can be used to receive the signal of MVB line A from the MVB bus of the second network segment, and convert the received MVB signal into a logic signal of, for example, 5V. At the same time, the RS-485 transceiver 122A drives the forwarding signal from the FPGA module 140A into an RS-485 signal and sends it to line A of the MVB bus of the second network segment.
Analyst Comments: *(**Note: X** – Represents that this reference when taken alone, the claimed invention cannot be considered*	*This patent application broadly discloses*

novel or cannot be considered to involve an inventive step; and Y - Represents that this reference can be relevant if combined with one or more references, such combination forms obviousness to a person skilled in the art)	

Back to Analysis Summary

Publication No.	**CN112684780A**		
Title	Control panel interface assembly for railway locomotive		
Assignee/Applicant	Zhengzhou Railway Vocational & Technical College		
Earliest Priority Date	2021-01-29	**Publication Date**	2021-04-20

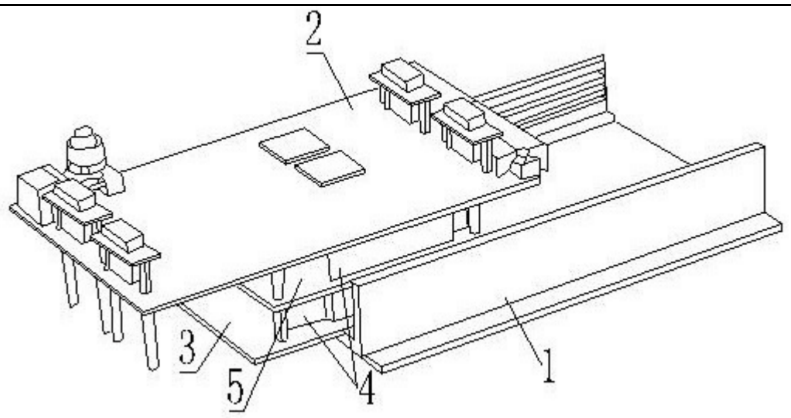
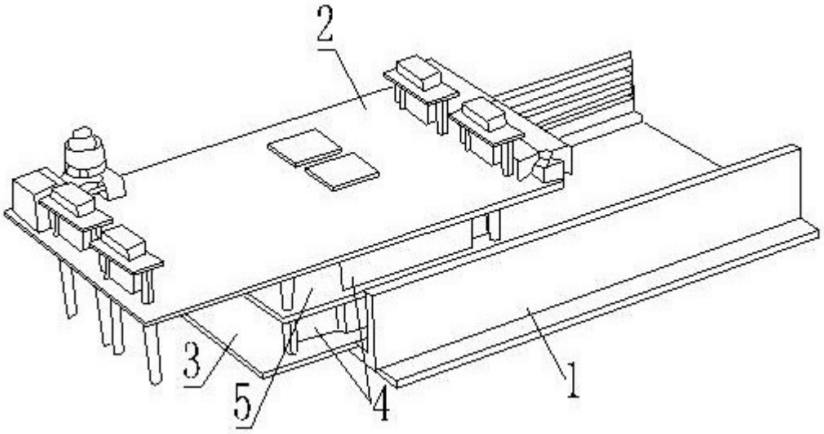
Abstract

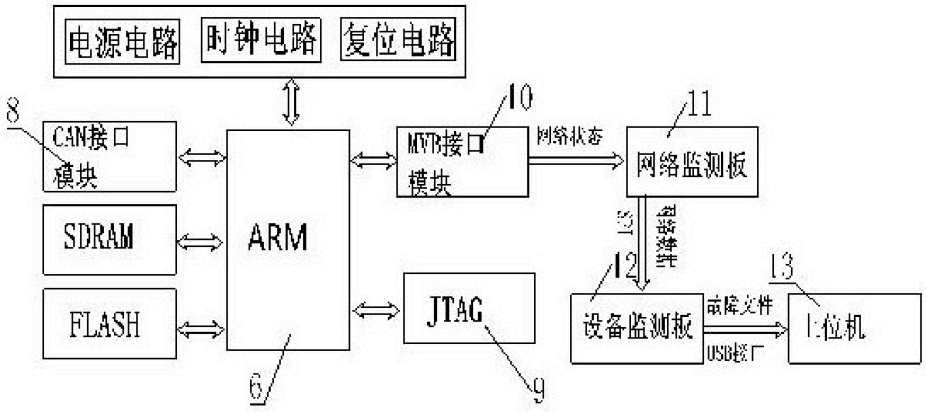
The invention relates to a control panel interface assembly for a railway locomotive. The assembly comprises a base, a CPU board card and a power supply board card, the CPU board card comprises an ARM processor, a communication module, a CAN interface module, an MVB interface module and a JTAG interface, wherein the MVB interface module is connected with a monitoring unit through an MVB bus. The monitoring unit comprises a network monitoring board and an equipment monitoring board which are connected to the MVB interface module through the MVB bus, data is transmitted between the network monitoring board and the equipment monitoring board through an SPI bus, and the equipment monitoring board is connected to an upper computer through a USB interface. The control panel interface assembly provided by the invention monitors the state and network data of main electrical equipment on the locomotive, and can record the state information and network transmission data of the equipment in a period of time before and after the fault when the equipment has the fault, thereby providing a basis for locomotive fault diagnosis and analysis, and providing a basis for locomotive overhaul and maintenance.

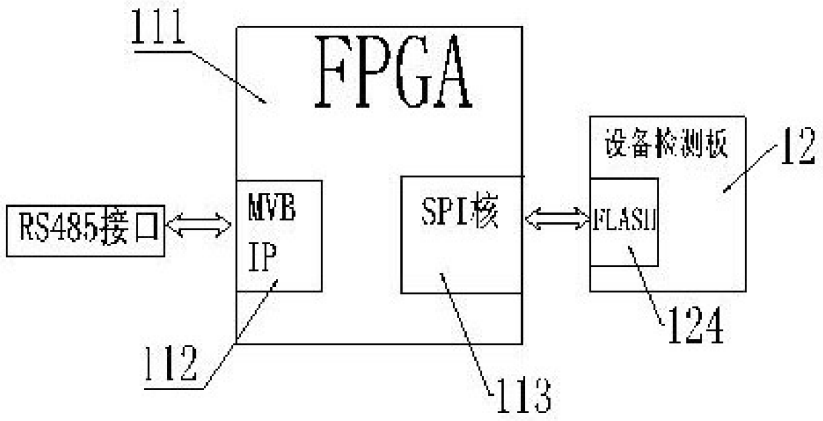
Description

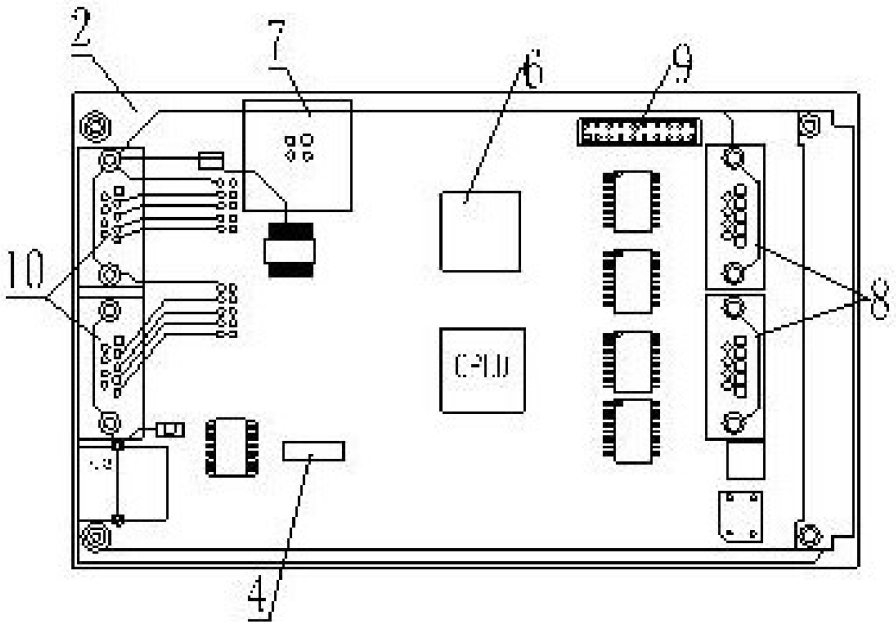
[Page 3]

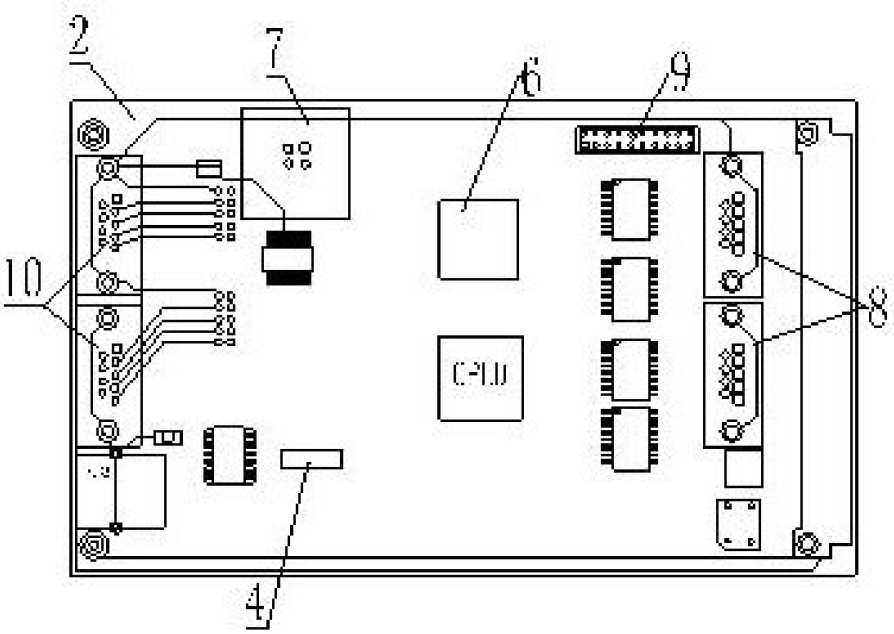
A control panel interface component for a railway locomotive comprises a base, a CPU board arranged above the base, and an MVB network card and a power board arranged on one side of the base, wherein the CPU board comprises an ARM processor, a communication module, a CAN interface module, an MVB interface module and a JTAG interface, the MVB interface module is connected to a monitoring unit via an MVB bus, the monitoring unit comprises a network monitoring board and an equipment monitoring board connected to the MVB interface module via the MVB bus, data is transmitted between the network monitoring board and the equipment monitoring board via an SPI bus, and the equipment monitoring board is connected to a host computer via a USB interface to realize communication with hardware equipment and perform online monitoring and analysis of locomotive faults.

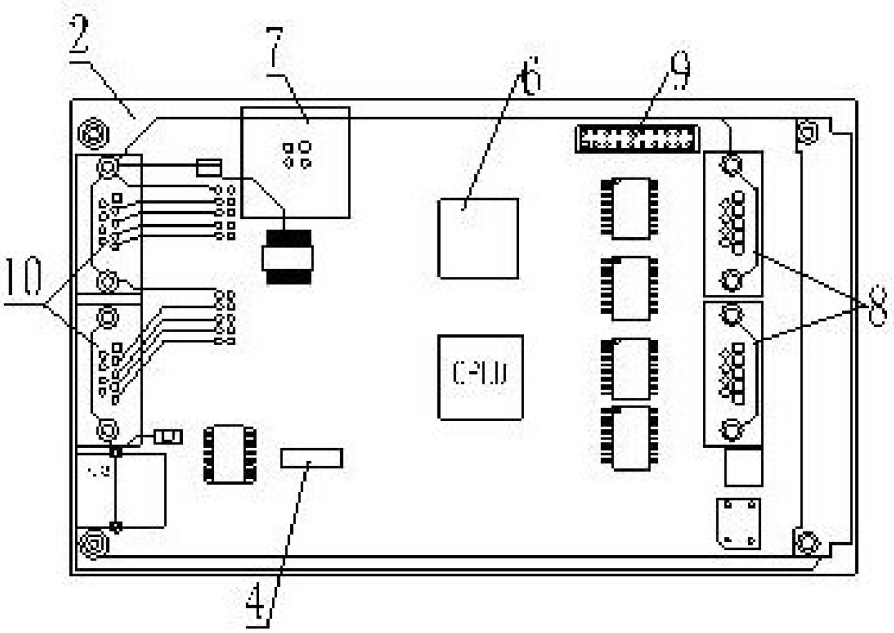
	 图1
	Description **[Page 11]** In conjunction with Figures 3-5, **the MVB interface module 10 is connected to a monitoring unit via an MVB bus. The monitoring unit includes a network monitoring board 11 and a device monitoring board 12 connected to the MVB interface module 10 via the MVB bus. Data is transmitted between the network monitoring board 11 and the device monitoring board 12 via the SPI bus.** The device monitoring board 12 is connected to a host computer 13 via a USB interface to achieve communication with hardware devices and perform online monitoring and analysis of locomotive faults.  图1 **[Page 12]**

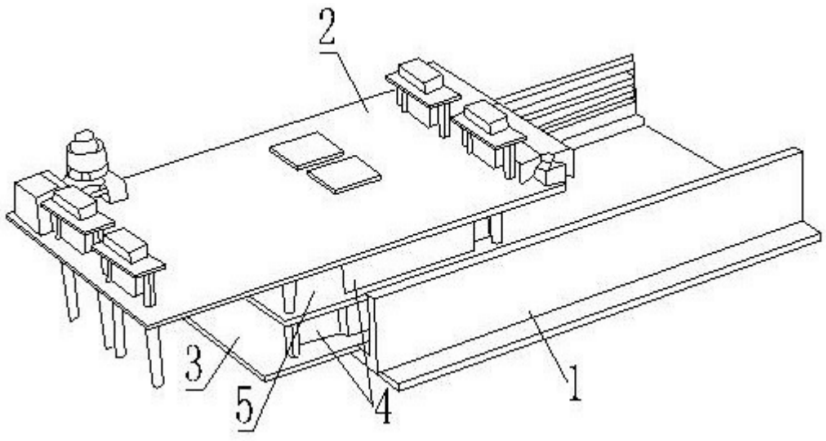
	The network monitoring board 11 includes: **an FPGA chip 111, including an MVB IP core 112 that implements the network link layer of the MVB interface module 10, which receives the transmitted process data and message data from the MVB bus, and caches them in the ARM processor 6 through the RS485 interface after decoding**; an SPI core 113, which is connected to the FLASH storage module 124 of the device monitoring board 12 to complete the data transmission between the device monitoring board 12.  图3
	[Page 12] The network monitoring board 11 includes: **an FPGA chip 111, including an MVB IP core 112 that implements the network link layer of the MVB interface module 10, which receives the transmitted process data and message data from the MVB bus, and caches them in the ARM processor 6 through the RS485 interface after decoding**; an SPI core 113, which is connected to the FLASH storage module 124 of the device monitoring board 12 to complete the data transmission between the device monitoring board 12.

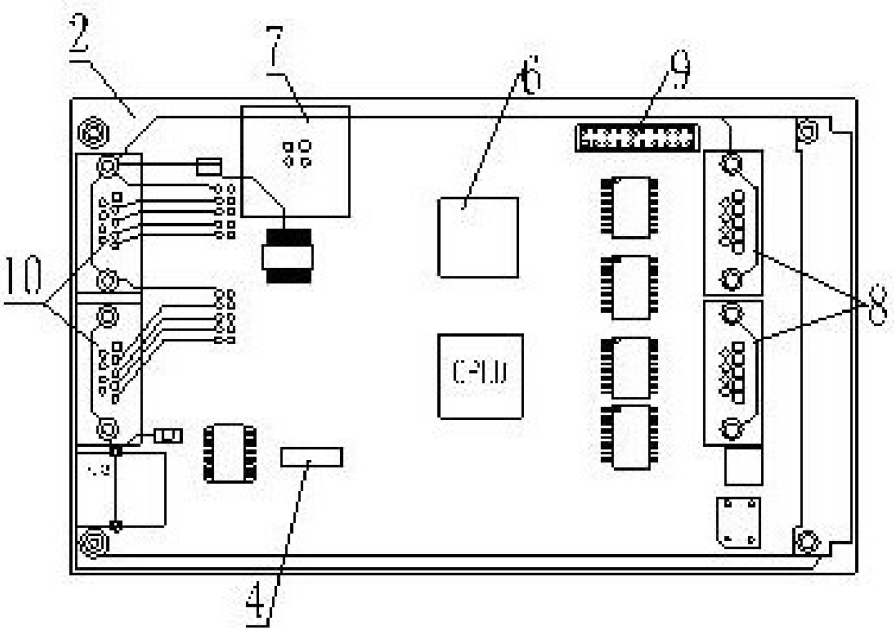
	 图5
	Description **[Page 10]** The CPU board configures the bus controller MVBC in the MVB network card through the PC/104 interface. **The bus controller MVBC is connected to the MVB communication medium through the bus transceiver manager and the isolation transformer to receive and transmit MVB data. The CPU board controls the CAN controller through the internal bus and then connects to the CAN communication medium through the CAN transceiver to receive and transmit CAN data.** The main controller CPU in the CPU board realizes the mutual conversion and storage of MVB and CAN bus data. The CPU accesses the PC/104 interface in I/O mode through the CPLD timing control.
	Description **[Page 7]** Preferably, the power board adopts an input lightning surge protection circuit, a secondorder common-mode filter circuit, **a first-order differential-mode filter circuit, a rectifier circuit, an output first-order common-mode filter circuit and a voltage stabilization circuit to reduce interference to the power circuit during locomotive travel and improve the reliability of the power supply.**

	 图2 **[Page 10]** **The base 1 adopts a box structure, uses U-shaped aluminum and is oxidized.** The board design adopts a 3U structure. The boards are connected using a PC/104 interface. Each connector uses a dedicated connector to ensure reliable connection and the casing is grounded through a capacitor. **The power board adopts an input lightning surge protection circuit, a second-order common-mode filter circuit, a first-order differential-mode filter circuit, a rectifier circuit, an output first-order common-mode filter circuit and a voltage stabilizing circuit to reduce interference to the power circuit during locomotive travel and improve the reliability of the power supply.**
	Description **[Page 3]** **Preferably, the base and the power board, the base and the MVB network card, and the base and the CPU board are connected via connectors respectively, and the connectors are PC /104 connectors.** **[Page 9]**

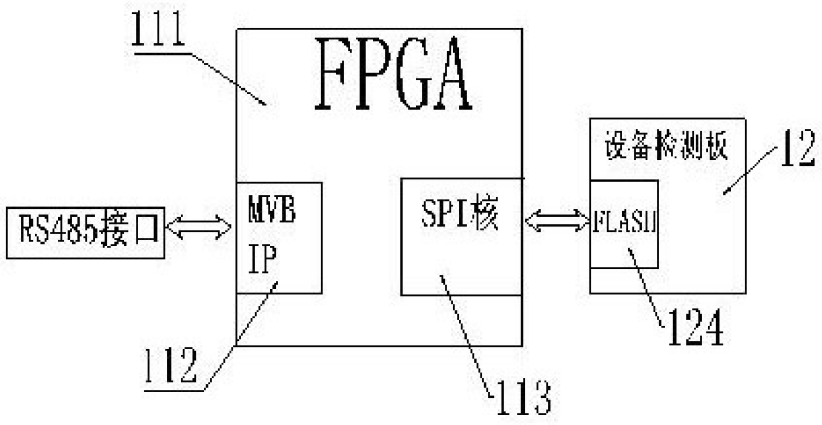
	In conjunction with Figures 1 and 2, a control panel interface assembly for a railway locomotive includes a base 1, **a CPU board 2 arranged above the base 1, and an MVB network card 5 and a power board 3 arranged on one side of the base 1. The base 1 and the power board 3, the base 1 and the MVB network card 5, and the base 1 and the CPU board 2 are connected respectively through connectors 4, and the connector 4 is a PC/104 connector.**  图2
	Description **[Page 3]** Preferably, the CPU board also includes an expansion module, and the expansion module includes **a power supply circuit, a clock circuit and a reset circuit.** **[Page 4]** DSP processor, responsible for monitoring the equipment operation status and the collection, **fault judgment and storage of fault data, and real-time clock to record the fault time;** **[Page 11]**

	It uses ARM processor as the center, and the periphery includes CAN interface module, MVB interface module, JTAG interface, power circuit, **clock circuit and reset circuit, SDRAM and FLASH memory module, which are used to enhance the driving ability of the bus, thereby increasing the communication distance of the CAN bus and allowing more nodes to be connected to the bus. During the operation of the gateway, CAN and MVB data can be quickly converted to achieve data interconnection and communication, ensuring a very short delay or even almost no delay. During the data conversion process, the accuracy and reliability of the data conversion are ensured; during the data transmission process, it is ensured that the data is not accumulated or lost. Make the gateway work normally and smoothly**
	Description **[Page 7]** Preferably, the power board adopts an input lightning surge protection circuit, a secondorder common-mode filter circuit, **a first-order differential-mode filter circuit, a rectifier circuit, an output first-order common-mode filter circuit and a voltage stabilization circuit to reduce interference to the power circuit during locomotive travel and improve the reliability of the power supply.**  图2

	[Page 10] The base 1 adopts a box structure, uses U-shaped aluminum and is oxidized. The board design adopts a 3U structure. The boards are connected using a PC/104 interface. Each connector uses a dedicated connector to ensure reliable connection and the casing is grounded through a capacitor. **The power board adopts an input lightning surge protection circuit, a second-order common-mode filter circuit, a first-order differential-mode filter circuit, a rectifier circuit, an output first-order common-mode filter circuit and a voltage stabilizing circuit to reduce interference to the power circuit during locomotive travel and improve the reliability of the power supply.**
	-
	[Page 10] **The base 1 adopts a box structure, uses U-shaped aluminum and is oxidized.** The board design adopts a 3U structure. The boards are connected using a PC/104 interface. Each connector uses a dedicated connector to ensure reliable connection and the casing is grounded through a capacitor. **The power board adopts an input lightning surge protection circuit, a second-order common-mode filter circuit, a first-order differential-mode filter circuit, a rectifier circuit, an output first-order common-mode filter circuit and a voltage stabilizing circuit to reduce interference to the power circuit during locomotive travel and improve the reliability of the power supply.**  图1 **[Page 7]**

	Preferably, the power board adopts an input lightning surge protection circuit, a secondorder common-mode filter circuit, **a first-order differential-mode filter circuit, a rectifier circuit, an output first-order common-mode filter circuit and a voltage stabilization circuit to reduce interference to the power circuit during locomotive travel and improve the reliability of the power supply.**  图2 **[Page 10]** The base 1 adopts a box structure, uses U-shaped aluminum and is oxidized. The board design adopts a 3U structure. The boards are connected using a PC/104 interface. Each connector uses a dedicated connector to ensure reliable connection and the casing is grounded through a capacitor. **The power board adopts an input lightning surge protection circuit, a second-order common-mode filter circuit, a first-order differential-mode filter circuit, a rectifier circuit, an output first-order common-mode filter circuit and a voltage stabilizing circuit to reduce interference to the power circuit during locomotive travel and improve the reliability of the power supply.**
	Description **[Page 6]**

	Preferably, **the CAN interface module is connected to a CAN acquisition module, which is responsible for collecting CAN real-time data and GPS data, performing data preprocessing, system parameter configuration transfer, and transmitting real-time data to a host computer and to a remote monitoring center via a 3G wireless router.** **[Page 7]** The present invention provides a control panel interface component for railway locomotives. The core of the signal acquisition and processing of the equipment fault monitoring board is DSP, which performs fault judgment by collecting the electrical status of the fault-related signal of the locomotive terminal block. **The core of the signal acquisition and processing of the network data monitoring board is FGPA, which receives the network data on the MVB bus in real time. When a device fails, the system can record the device status and network transmission data before and after the failure, and store the data in the FLASH of the equipment monitoring board in the form of a fault file.** After getting off the vehicle, the fault file can be copied to the host computer by connecting to the host computer, and offline fault data analysis and fault diagnosis can be achieved through the host computer analysis software. **[Page 11]** The equipment monitoring board 12 includes: a DSP processor 121, which takes the **DSP processor as the core processing unit and is responsible for monitoring the equipment operation status and the collection, fault judgment, and fault data storage of fault data, and a real-time clock to record the fault time;** a CPLD logic decoding module 123, which decodes the address of the expansion device and generates the corresponding timing of each hardware; an SDRAM data cache module 122, which serves as a dynamic cache for the system operation; and a FLASH storage module 124, which stores fault data in large capacity. **[Page 12]** **The CAN interface module is connected to the CAN acquisition module, which is responsible for collecting CAN real-time data and GPS data, performing data preprocessing, system parameter configuration transfer, and transmitting real-time data to the host computer at the same time, and transmitting real-time data to the remote monitoring center through the 3G wireless router.** The CAN acquisition module includes a 3G wireless router, a GPS module, a switch, a power module and a

	battery. The base adopts a double-layer parallel arrangement structure, with a 3G wireless router and a switch placed on the upper layer of the base, and a CPU board, a power module, and a GPS module placed on the lower layer of the base. A partition is provided at the inner bottom end of the base, and a battery is placed in the partition.
	Description **[Page 10]** **The MVB network card includes: MVBC, which completes sending the data bytes to be sent to the transmission medium through the serialization circuit, and realizes the conversion of serial data on the MVB bus into parallel data bytes; communication memory, which stores all data and information of MVBC; physical layer interface, which is connected to the MVB network card 5 in the form of an electrical short-distance medium ESD+ interface, and is photoelectrically isolated from the outside world by optical coupling to improve system reliability.** **[Page 12]** **The network monitoring board 11 includes: an FPGA chip 111, including an MVB IP core 112 that implements the network link layer of the MVB interface module 10, which receives the transmitted process data and message data from the MVB bus, and caches them in the ARM processor 6 through the RS485 interface after decoding; an SPI core 113, which is connected to the FLASH storage module 124 of the device monitoring board 12 to complete the data transmission between the device monitoring board 12.**  图5
Analyst Comments:	*This patent application broadly discloses*

*(**Note: X** – Represents that this reference when taken alone, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step; and Y - Represents that this reference can be relevant if combined with one or more references, such combination forms obviousness to a person skilled in the art)*	

Back to Analysis Summary

Publication No.	CN104361652A		
Title	Data recording device of network control and monitoring system of train		
Assignee/Applicant	Csr Zhuzou Electric Locomotive Res Inst Co. Ltd.		
Earliest Priority Date	2014-11-12	Publication Date	2015-02-18

Abstract

The invention discloses a data recording device of a network control and monitoring system of a train, belonging to the technical field of rail transportation. The data recording device can adapt to severe environments of vibration, high temperature and the like during running of the train, and has the advantages of simple structure, low cost, large storage capacity, relatively high reliability and the like. The data recording device of the network control and monitoring system of the train comprises a CPU unit, an interface unit, a logical unit and a storage unit, wherein the CPU unit is connected with the interface unit, the logical unit and the storage unit respectively; the interface unit is used for receiving data from the network control and monitoring system of the train and comprises an MVB bus interface module and an MVB bus control module, and the MVB bus control module is connected with the CPU unit and is used for monitoring the MVB bus interface module; the logical unit is used for adjusting the time sequence of the MVB bus control module to ensure that the time sequence of the MVB bus control module is matched with that of the CPU unit; and the storage unit comprises a CF card for storing the data from the network control and monitoring system of the train.

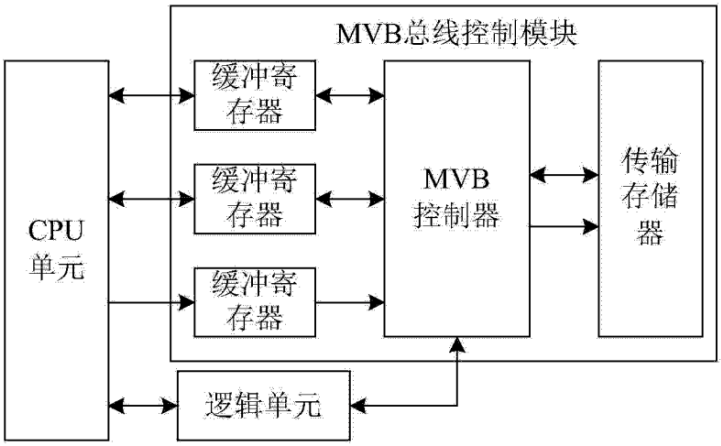
Description

[Page 3]

Wherein, the interface unit is used to access data from the train network control and monitoring system, and **includes an MVB bus interface module and an MVB bus control module, and the MVB bus control module is connected to the CPU unit and is used to monitor the MVB bus interface module;**

[Page 4]

The present invention brings the following beneficial effects: An embodiment of the present invention provides a data recording device for a train network control and monitoring system, the data recording device comprising a CPU unit, an interface unit, a logic unit and a storage unit. **The interface unit includes an MVB bus interface module and an MVB bus control module connected to the CPU unit and used to monitor the MVB bus interface module; the logic unit is used to adjust the timing of the MVB**

	bus control module in the MVB bus interface module so that the timing of the MVB bus control module matches that of the CPU unit, and the storage unit includes a CF card. The data recording device can match the commonly used MVB bus interface module with the CPU unit and use a CF card for storage. It can adapt to harsh environments such as vibration and high temperature during train operation, and has the advantages of simple structure, low cost, large storage capacity and high reliability.  图 4
	Description **[Page 3]** Among them, **the MVB bus interface module includes two MVB bus interface circuits, the two MVB bus interface circuits are redundant to each other, and the MVB bus control module is specifically used to monitor and switch the two MVB bus interface circuits.**
	Description **[Page 8]** As shown in Figure 3, **the FPGA chip is connected to the central processing unit of the CPU unit through a local bus, and can control key signals such as chip selection, interrupt, input /output (IO) of the central processing unit. The FPGA chip has the function of adjusting the timing of the MVB bus control module, thereby solving the problem of mismatch between the control timing of the MVB bus control module and the CPU unit. At the same time, the FPGA chip can also control the key signals of the MVB bus control module, such as interrupt, reset, read and write, and chip select.**

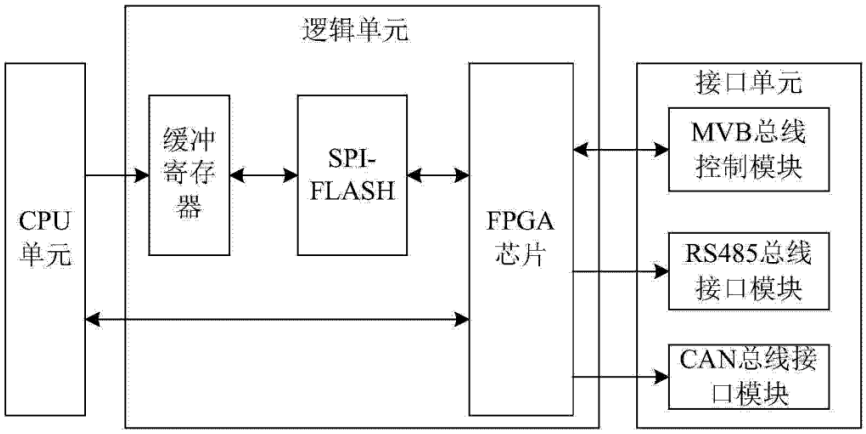


图 3

[Pages 9-10]

As shown in Figure 4, in an embodiment of the present invention, three signal lines are arranged between the MVB bus control module and the CPU unit, two of which are used to transmit data signals and are bidirectional signal lines, and the remaining one signal line is used to transmit address signals and is a unidirectional signal line, and buffer registers are arranged on the three signal lines. The MVB bus control module also includes an MVB controller and transmission memory (Transmission Memmory, TM for short). Any signal line of the MVB bus control module is connected to the TM and buffer register via a parallel bus. As shown in FIG3 , when the central processing unit in the CPU unit wants to write data to the MVB bus control module, it first sends a write signal to the MVB bus control module through the FPGA chip in the logic unit. **After receiving the write signal, the MVB controller in the MVB bus control module immediately returns a confirmation signal through the FPGA chip, and then controls the buffer register to temporarily store the data in the TM. After all data from the CPU unit has been stored, the temporarily stored data can be read from the TM. When the MVB controller in the MVB bus control module sends data to the CPU unit, it first temporarily writes the data into the TM, and then sends a relevant signal to the CPU unit through the FPGA chip. After receiving the relevant signal, the CPU unit can read out the data temporarily stored in the TM with the assistance of the MVB bus control module.**

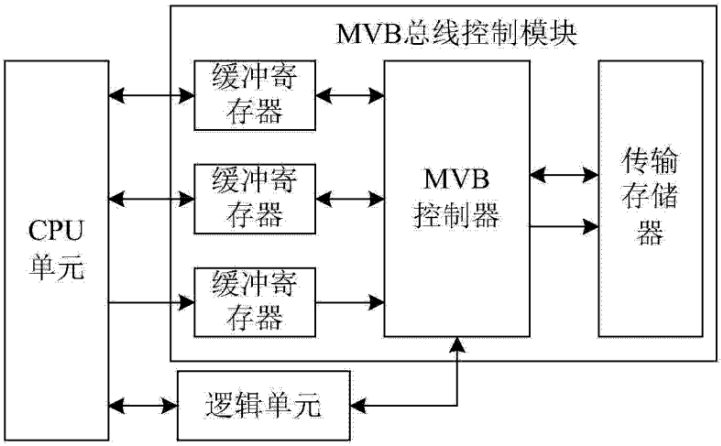


图 4

Description

[Page 11]

Specifically, as shown in FIG7 , **the RS485 bus interface module is composed of two identical RS485 bus interface circuits, and each RS485 bus interface circuit is composed of three optical couplers, an RS485 transceiver and a connector (eg, a DB9 connector).** The isolated power supply can provide 5V DC voltage for the RS485 transceiver and connector structures in each RS485 bus interface circuit.

At the same time, **the isolated power supply is also beneficial to protect the various structures in the RS485 bus interface circuit from external pulse shocks, which can improve the protection capability of the RS485 bus interface circuit and reduce the damage to the data recording device caused by external interference.**

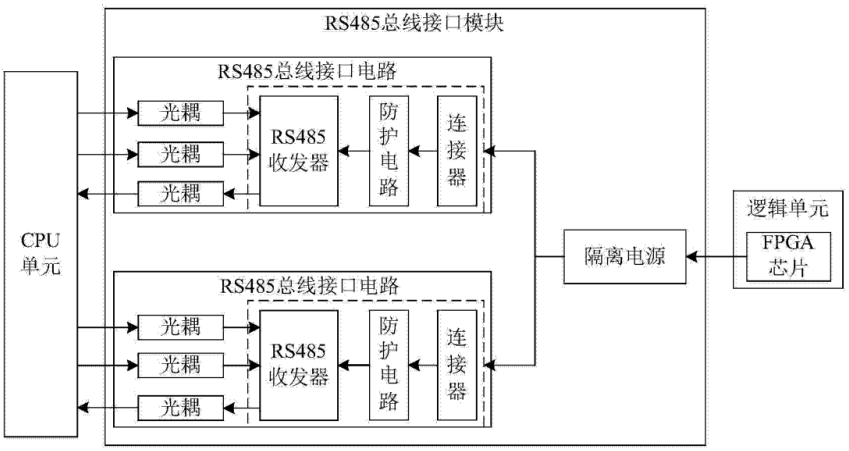
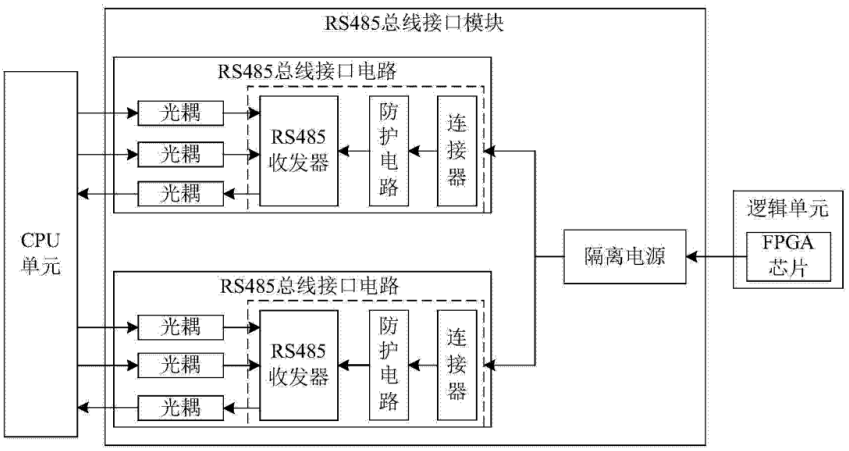
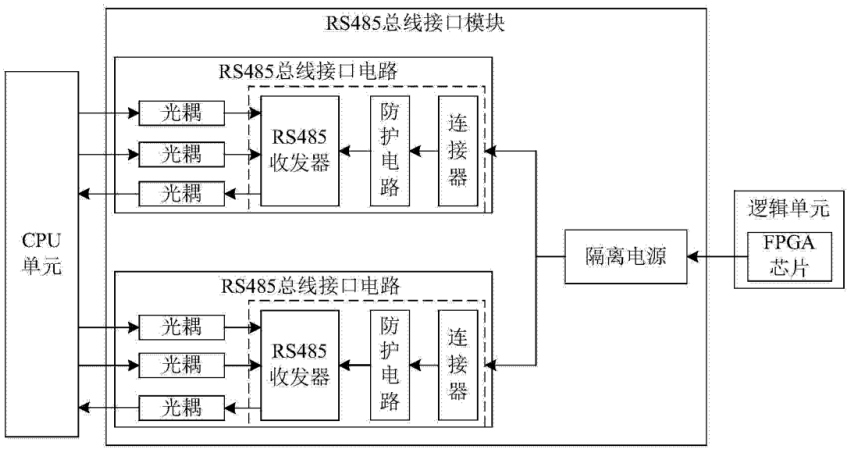


图 7

	[Page 12] **In order to better prevent interference on the external communication line from affecting the internal circuit of the data recording device, three optocouplers are added between the RS485 transceiver and the CPU unit of the RS485 bus interface circuit.** The three optocouplers can electrically isolate the signals, and the isolation voltage of the optocouplers can reach 3750V.
	Description **[Page 3]** **Wherein, the logic unit includes a buffer register,** a flash memory circuit and an FPGA chip, the flash memory circuit is used to store the configuration program of the FGPA chip, and the FGPA chip is used to adjust the timing of the MVB bus control module**.** **[Page 11]** Specifically, as shown in FIG7 , **the RS485 bus interface module is composed of two identical RS485 bus interface circuits, and each RS485 bus interface circuit is composed of three optical couplers, an RS485 transceiver and a connector (eg, a DB9 connector).** The isolated power supply can provide 5V DC voltage for the RS485 transceiver and connector structures in each RS485 bus interface circuit. At the same time, **the isolated power supply is also beneficial to protect the various structures in the RS485 bus interface circuit from external pulse shocks, which can improve the protection capability of the RS485 bus interface circuit and reduce the damage to the data recording device caused by external interference.**  图 7

	[Page 12] **In order to better prevent interference on the external communication line from affecting the internal circuit of the data recording device, three optocouplers are added between the RS485 transceiver and the CPU unit of the RS485 bus interface circuit. The three optocouplers can electrically isolate the signals, and the isolation voltage of the optocouplers can reach 3750V.**
	Description **[Page 3]** **Wherein, the data recording device also includes a power module, and the power module supplies power to the CPU unit, the interface unit, the logic unit and the storage unit.** **[Page 11]** Specifically, as shown in FIG7 , **the RS485 bus interface module is composed of two identical RS485 bus interface circuits, and each RS485 bus interface circuit is composed of three optical couplers, an RS485 transceiver and a connector (eg, a DB9 connector). The isolated power supply can provide 5V DC voltage for the RS485 transceiver and connector structures in each RS485 bus interface circuit.** At the same time, the isolated power supply is also beneficial to protect the various structures in the RS485 bus interface circuit from external pulse shocks, which can improve the protection capability of the RS485 bus interface circuit and reduce the damage to the data recording device caused by external interference.  图 7

Description

[Page 7]

The CPU unit is the core of the entire data recording device, which is responsible for processing, calculating, allocating storage and controlling communication of data. As shown in Figure 2, **the CPU unit specifically includes a central processing unit and a double data rate synchronous dynamic random access memory (DDR) circuit, a flash memory (FLASH) circuit, a watchdog circuit, a clock circuit, a JTAG interface circuit, a function configuration circuit and a temperature control module that are arranged and connected around it. The DDR circuit consists of two 16-bit DDR chips, realizing 64M and 32-bit storage functions. The external clock circuit includes an oscillator and a crystal, which provide the system clock and real-time clock for the central processing unit respectively.** The FLASH circuit includes two FLASH chips, and its data write protection function is controlled by the logic unit. The watchdog circuit can monitor external programs and the two power supply voltages of the central processing unit. It also has the functions of power-on, reset, and delay. The JTAG interface circuit supports functions such as program downloading, single-step instruction execution, setting and observing program breakpoints, and observing the internal register status of the CPU unit. The temperature monitoring module is composed of a temperature sensor, which is connected to the central processing unit through a two-wire serial (Inter-Integrated Circuit, abbreviated as I2C) bus. It is used to monitor the temperature of the data recording device and send out an alarm signal when it is determined that the temperature of the data recording device exceeds the preset temperature value.

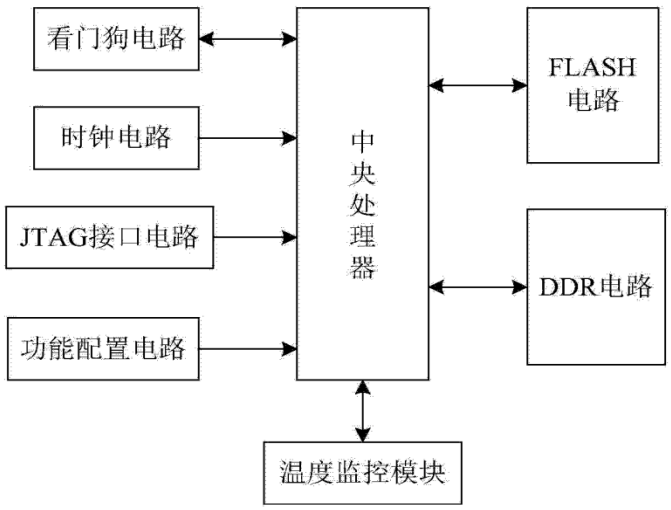
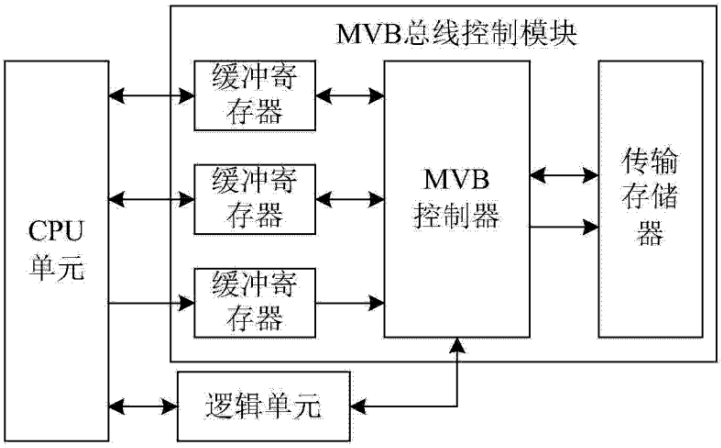
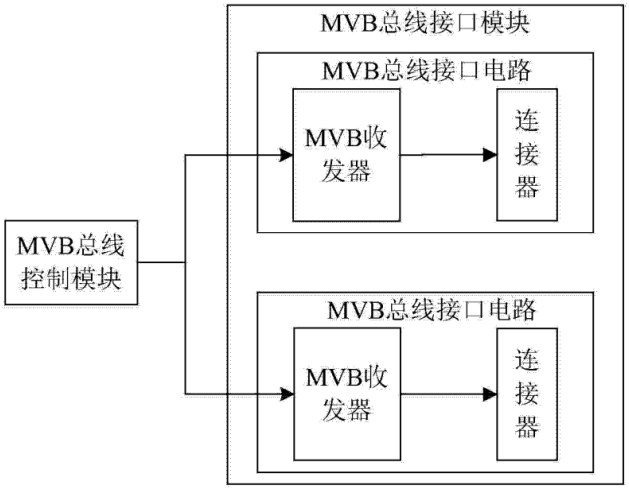


图 2

	Description **[Page 10]** Furthermore, in addition to the above units, the data recording device disclosed in the embodiment of the present invention also includes a power module, which supplies power to the CPU unit, the interface unit, the logic unit and the storage unit. **Specifically, the power module converts the vehicle's 110V power input into a 5V DC voltage output to power each unit.**
	Description **[Page 4]** The present invention brings the following beneficial effects: An embodiment of the present invention provides a data recording device for a train network control and monitoring system, the data recording device comprising a CPU unit, an interface unit, a logic unit and a storage unit. **The interface unit includes an MVB bus interface module and an MVB bus control module connected to the CPU unit and used to monitor the MVB bus interface module; the logic unit is used to adjust the timing of the MVB bus control module in the MVB bus interface module so that the timing of the MVB bus control module matches that of the CPU unit, and the storage unit includes a CF card. The data recording device can match the commonly used MVB bus interface module with the CPU unit and use a CF card for storage. It can adapt to harsh environments such as vibration and high temperature during train operation, and has the advantages of simple structure, low cost, large storage capacity and high reliability.**  图 4
	-

	Description **[Page 2]** **Wherein, the interface unit is used to access data from the train network control and monitoring system,** and includes an MVB bus interface module and an MVB bus control module, and the MVB bus control module is connected to the CPU unit and is used to monitor the MVB bus interface module; **[Page 3]** Wherein, the interface unit is used to access data from the train network control and monitoring system, and **includes an MVB bus interface module and an MVB bus control module, and the MVB bus control module is connected to the CPU unit and is used to monitor the MVB bus interface module;** **[Page 4]** Wherein, the CPU unit includes a temperature monitoring module for monitoring the temperature of the data recording device, and **when it is determined that the temperature of the data recording device exceeds a preset temperature value, an alarm signal is issued.**
	Description **[Page 3]** **Wherein, the interface unit is used to access data from the train network control and monitoring system, and includes an MVB bus interface module and an MVB bus control module, and the MVB bus control module is connected to the CPU unit and is used to monitor the MVB bus interface module;** **[Page 8]** As shown in Figure 3, the FPGA chip is connected to the central processing unit of the CPU unit through a local bus, and can control key signals such as chip selection, interrupt, input /output (IO) of the central processing unit. **The FPGA chip has the function of adjusting the timing of the MVB bus control module, thereby solving the problem of mismatch between the control timing of the MVB bus control module and the CPU unit. At the same time, the FPGA chip can also control the key signals of the MVB bus control module, such as interrupt, reset, read and write, and chip select.** **[Page 8]**

	As shown in Figure 4, in an embodiment of the present invention, three signal lines are arranged between the MVB bus control module and the CPU unit, two of which are used to transmit data signals and are bidirectional signal lines, and the remaining one signal line is used to transmit address signals and is a unidirectional signal line, and buffer registers are arranged on the three signal lines. The MVB bus control module also includes an MVB controller and transmission memory (Transmission Memmory, TM for short). **Any signal line of the MVB bus control module is connected to the TM and buffer register via a parallel bus. As shown in FIG3 , when the central processing unit in the CPU unit wants to write data to the MVB bus control module, it first sends a write signal to the MVB bus control module through the FPGA chip in the logic unit.** **[Page 9]** Furthermore, as shown in FIG5 , the MVB bus interface module includes two MVB bus interface circuits, and the two MVB bus interface circuits are redundant to each other. **The MVB bus control module in the embodiment of the present invention is specifically used to monitor and switch two MVB bus interface circuits. Specifically, each MVB bus interface circuit is composed of an MVB transceiver and a connector (such as a DB9 connector). The external device synchronously sends the same data on the two transmission lines corresponding to the two MVB bus interface circuits, while the MVB bus control module only receives data from the transmission line corresponding to one of the MVB bus interface circuits, which is called the trusted line.** The MVB bus control module also monitors the transmission line corresponding to the other MVB bus interface circuit, which is called the monitoring line. When the MVB transceiver in the MVB bus control module detects that the current trust line has timed out or the signal quality is poor, it will automatically switch to the monitoring line and use the current monitoring line as the trust line and the other line (the original trust line) as the monitoring line. This process is repeated to achieve switching between the two MVB bus interface circuits controlled by the MVB bus control module, so that the two MVB bus interface circuits can be redundant to each other.

	 图 5
Analyst Comments: *(**Note: X** – Represents that this reference when taken alone, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step; and Y - Represents that this reference can be relevant if combined with one or more references, such combination forms obviousness to a person skilled in the art)*	*This patent application broadly discloses*

Back to Analysis Summary

Publication No.	**CN220190895U**		
Title	Ethernet changes MVB gateway device		
Assignee/Applicant	CRRC Qingdao Sifang Rolling Stock Res Inst Co Ltd		
Earliest Priority Date	2023-06-05	**Publication Date**	2023-12-15

Abstract

The utility model relates to an Ethernet-to-MVB gateway device, which comprises: a case; install at the inside first circuit board of box, first circuit board includes: an ethernet interface, an ethernet interface circuit module electrically connected to the ethernet interface, and an embedded processor module electrically connected to the ethernet interface circuit module; install the inside second circuit board of box, the second circuit board includes: the system comprises an MVB interface, a transceiver electrically connected with the MVB interface, and an FPGA module electrically connected with the transceiver; the power supply module is electrically connected with the first circuit board and the second circuit board and is used for providing voltage for the embedded processor module and the FPGA module; the embedded processor module is electrically connected with the FPGA module; the utility model provides an Ethernet-to-MVB gateway device which can be adapted to any computer with an Ethernet interface and can accept an upper computer test case instruction to realize automatic test.

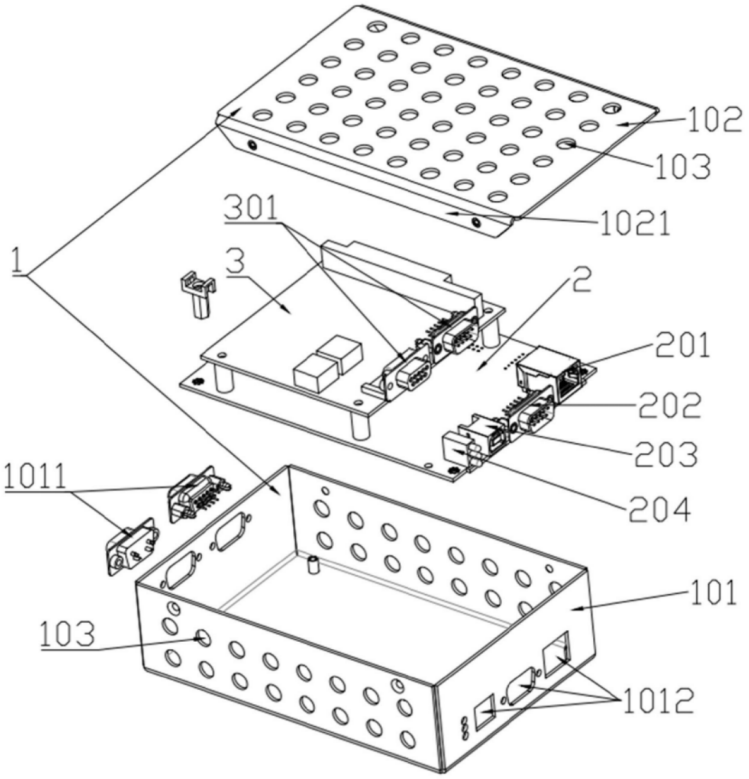
Description

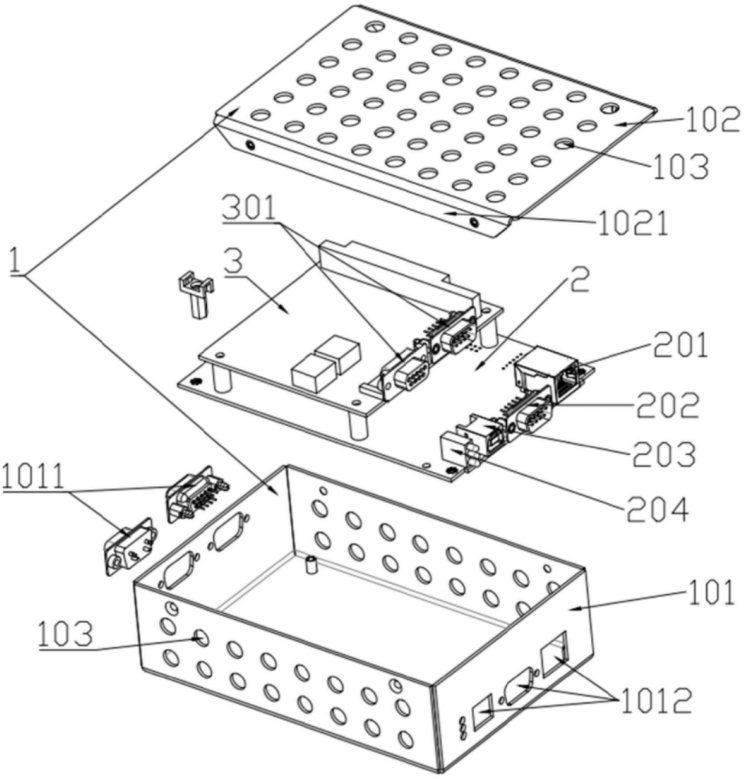
[Page 3]

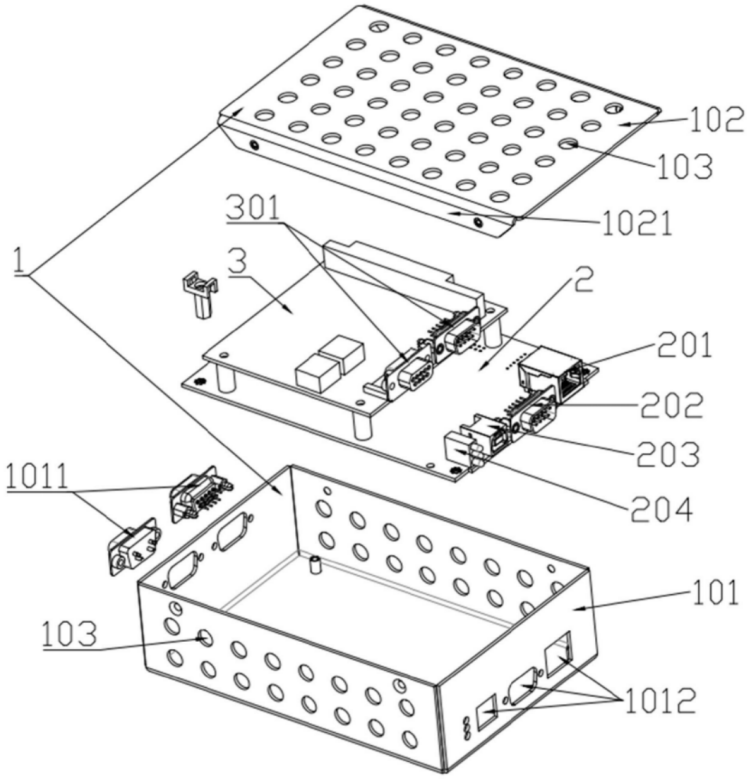
In some embodiments of the present invention**, the MVB interface and the transceiver are both provided in plurality, each of the MVB interfaces is electrically connected to one of the transceivers, and all of the transceivers are electrically connected to the FPGA module.**

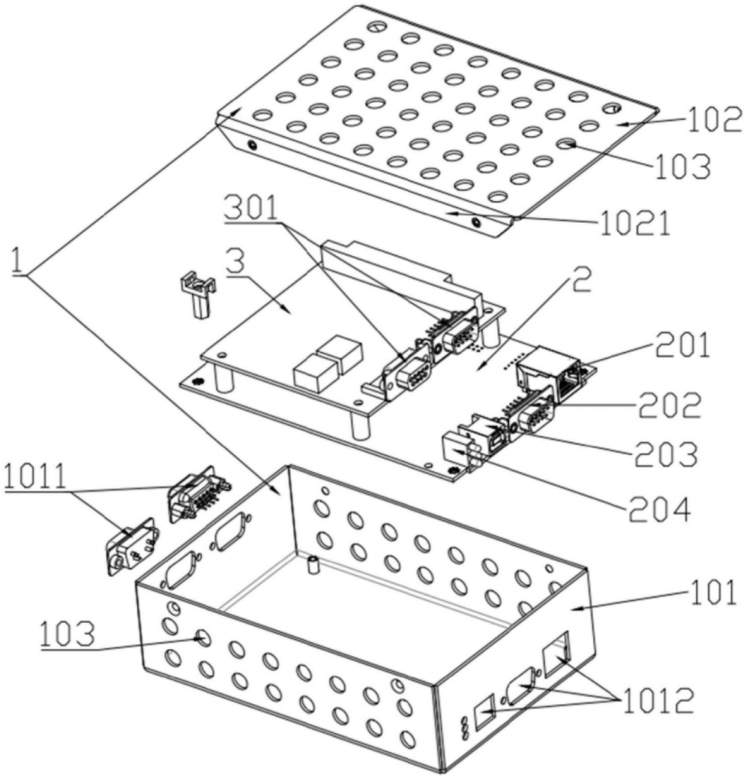
[Page 8]

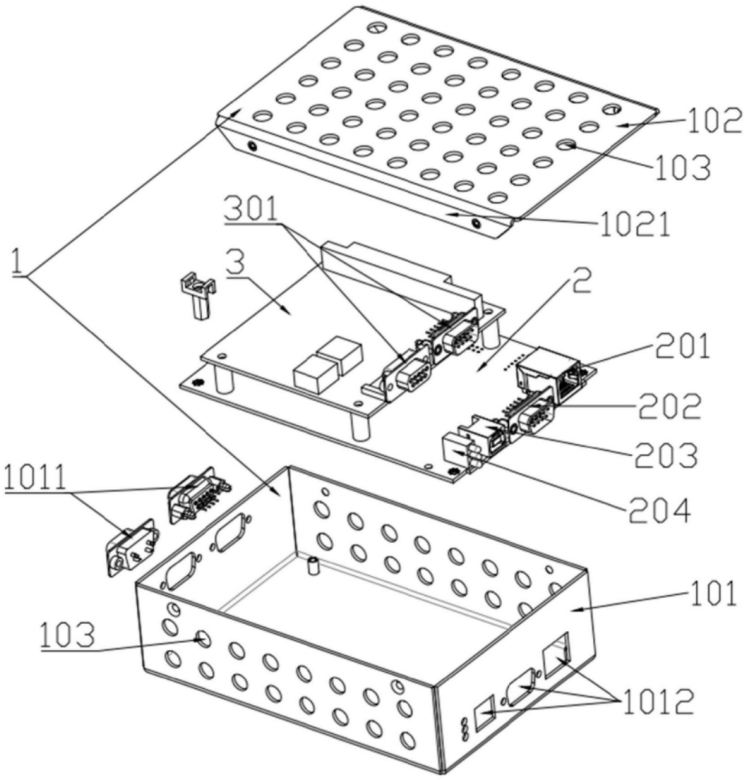
A second circuit board 3 installed inside the box 1, the second circuit board 3 includes: an MVB interface 301, a transceiver electrically connected to the MVB interface 301, and an FPGA module electrically connected to the transceiver;

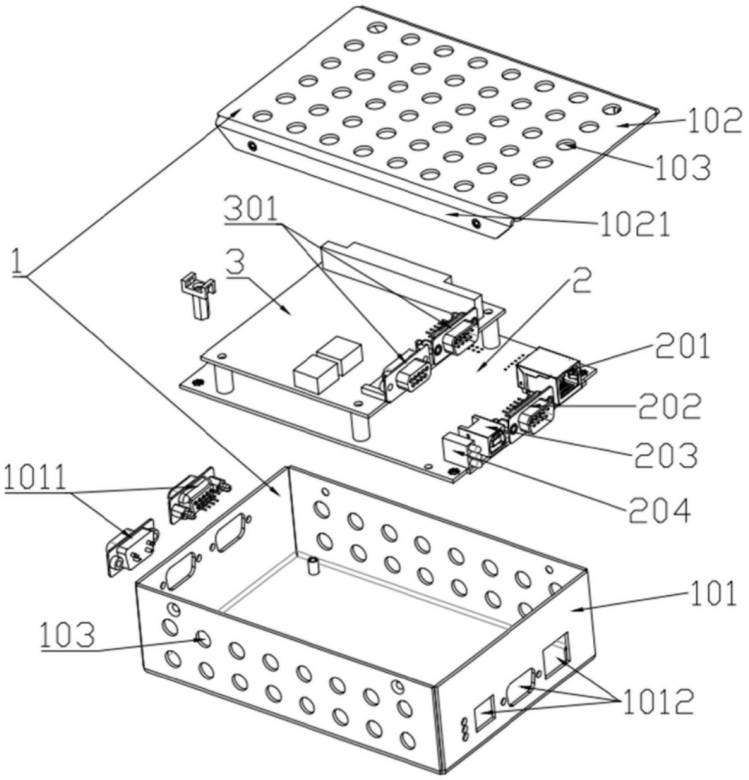
	 图2
	Description **[Page 3]** In some embodiments of the present invention**, the MVB interface and the transceiver are both provided in plurality, each of the MVB interfaces is electrically connected to one of the transceivers, and all of the transceivers are electrically connected to the FPGA module.** **[Page 8]** **A second circuit board 3 installed inside the box 1, the second circuit board 3 includes: an MVB interface 301, a transceiver electrically connected to the MVB interface 301, and an FPGA module electrically connected to the transceiver;**

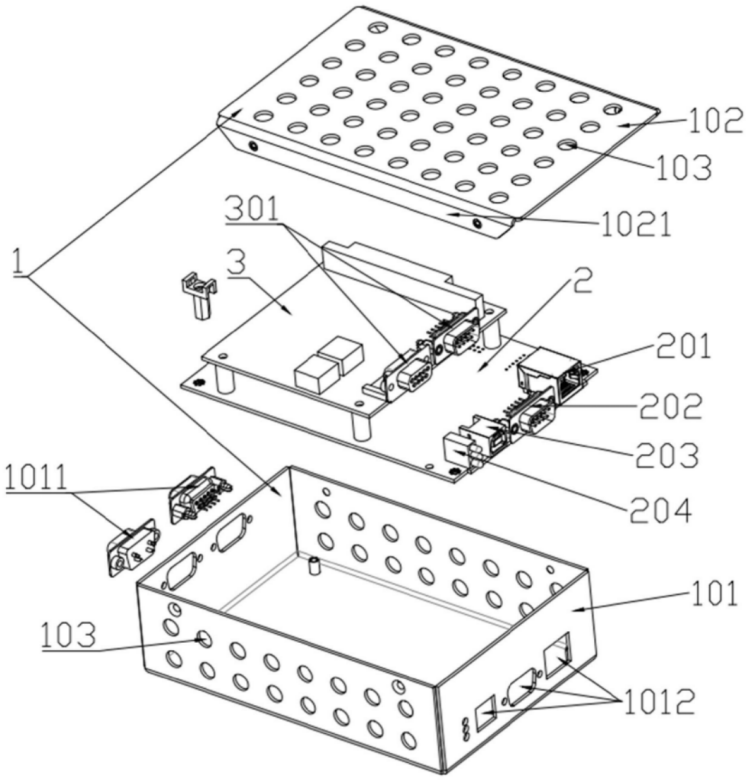
	 图2
	Description **[Page 8]** **A second circuit board 3 installed inside the box 1, the second circuit board 3 includes: an MVB interface 301, a transceiver electrically connected to the MVB interface 301, and an FPGA module electrically connected to the transceiver;**

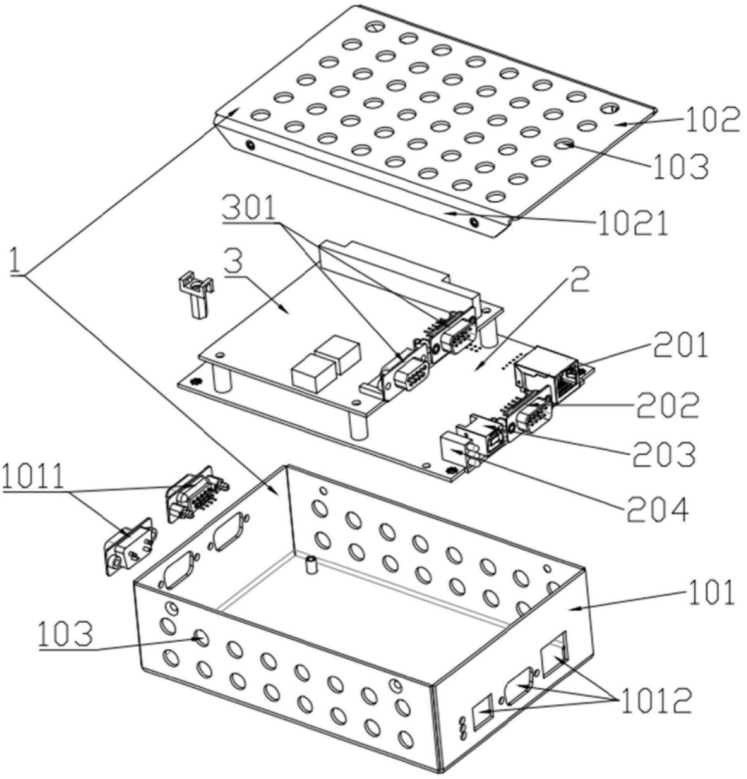
	 图2 **[Page 8]** **The embedded processor main control module is electrically connected to the FPGA module through the data bus and the address bus to complete the control and information exchange of each sub-module;** the second circuit board 3 and the MVB bus use the DB9 connecting line in half-duplex mode to communicate, which is used to receive the control signal of the first circuit board 2 and realize the conversion between RS485 level and TTL logic level; the first circuit board 2 is used to receive the signal transmitted by the external Ethernet device, send instructions after analysis, and transmit the control signal for setting the MVB port to the first circuit board 2. **[Page 11]** **The FPGA module sends the TTL level main frame data to the transceiver, and the transceiver converts the received TTL level main frame data into RS485 level data and sends it to the MVB bus.**
	Description **[Page 3]**

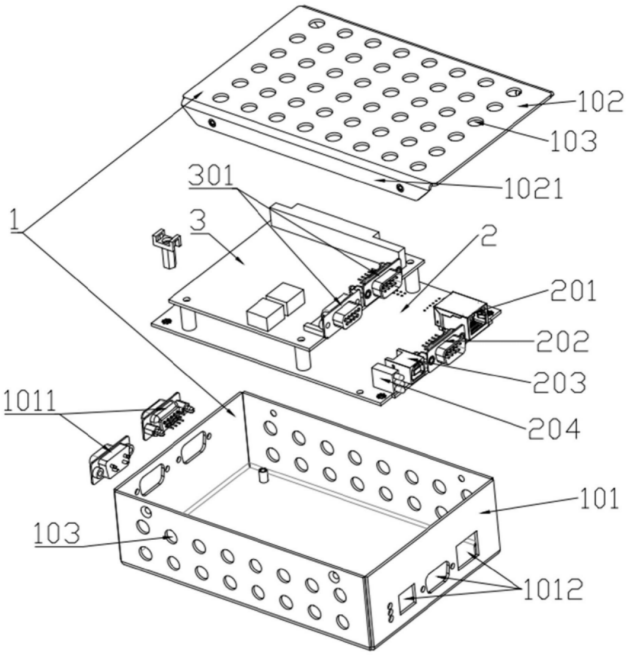
	A second circuit board is installed inside the box, and includes an MVB interface, an FPGA module, and a transceiver. The MVB interface is electrically connected to the transceiver, and the transceiver is electrically connected to the FPGA module. **[Page 8]** In some embodiments, **there are multiple MVB interfaces 301 and multiple transceivers, the number of transceivers corresponds to the number of MVB interfaces 301, each MVB interface 301 is electrically connected to a transceiver, and all transceivers are electrically connected to the FPGA module**. The MVB interface 301 is provided with a male connector and a female connector, and has a rich external interface, so that the utility model has an MVB redundancy function and is suitable for a variety of application scenarios.  图2 **[Page 9]** Furthermore, **the first circuit board 2 further includes an isolation circuit, each isolation circuit is electrically connected to one of the MVB interfaces 301** , and

	each isolation circuit is connected to at least one transceiver**. The isolation circuit reduces mutual interference between different circuits and reduces noise; and the connection form of the isolation circuit and the transceiver can further improve the redundancy of the device.**
	Description **[Page 9]** Furthermore, **the first circuit board 2 further includes an isolation circuit, each isolation circuit is electrically connected to one of the MVB interfaces 301** , and each isolation circuit is connected to at least one transceiver**. The isolation circuit reduces mutual interference between different circuits and reduces noise; and the connection form of the isolation circuit and the transceiver can further improve the redundancy of the device.**  图2
	Description **[Page 3]** **A power supply module, the power supply module comprising a USB interface and a power supply circuit module, the USB interface is electrically connected to the power supply circuit module, the power supply circuit module is**

	electrically connected to the first circuit board and the second circuit board, and provides voltage for the embedded processor module and the FPGA module; **[Page 8]** **The power supply module includes a USB interface 203 and a power supply circuit module electrically connected thereto. The power supply circuit module is electrically connected to the first circuit board 2 and the second circuit board 3 respectively to provide a 3.3V voltage for the embedded processor module and the FPGA module.**  图2
	-
	Description **[Page 9]**

	Furthermore, **the first circuit board 2 further includes an isolation circuit, each isolation circuit is electrically connected to one of the MVB interfaces 301** , and each isolation circuit is connected to at least one transceiver**. The isolation circuit reduces mutual interference between different circuits and reduces noise; and the connection form of the isolation circuit and the transceiver can further improve the redundancy of the device.**  图2
	Description **[Page 9]** **The outer shell 101 has a connector 1011 corresponding to the MVB interface 301 installed on one side thereof, and the connector 1011 is electrically connected to the MVB interface 301.** The other side of the outer shell 101 has signal ports 1012 corresponding to the Ethernet interface 201, the UART interface 202, and the USB interface 203, respectively, for leading out the circuit interface inside the box;

	 图2
	Description **[Page 9]** Furthermore, **the first circuit board 2 further includes an isolation circuit, each isolation circuit is electrically connected to one of the MVB interfaces 301** , and each isolation circuit is connected to at least one transceiver**. The isolation circuit reduces mutual interference between different circuits and reduces noise; and the connection form of the isolation circuit and the transceiver can further improve the redundancy of the device.**

	 图2 **[Page 10]** In some embodiments, as shown in FIG. 2 , **the outer shell body 101 and the outer shell cover 102 each have a plurality of heat dissipation holes 103 , the heat dissipation holes 103 on the front and rear surfaces of the outer shell body 101 are distributed in an array, and the heat dissipation holes 103 on the outer shell cover 102 are also distributed in an array.** The outer shell adopts a rigid porous structure with high heat dissipation efficiency, high hardness and is not easy to deform.
	-
	Description **[Page 2]** A first circuit board is installed inside the box, and the first circuit board includes: an Ethernet interface, **an Ethernet interface circuit module, and an embedded processor module, wherein the Ethernet interface is electrically connected to the Ethernet interface circuit module, and the Ethernet interface circuit module is electrically connected to the embedded processor module**; **[Page 3]**

	A second circuit board is installed inside the box, **and includes an MVB interface, an FPGA module, and a transceiver. The MVB interface is electrically connected to the transceiver, and the transceiver is electrically connected to the FPGA module.** **[Page 8]** In some embodiments, **there are multiple MVB interfaces 301 and multiple transceivers, the number of transceivers corresponds to the number of MVB interfaces 301, each MVB interface 301 is electrically connected to a transceiver, and all transceivers are electrically connected to the FPGA module. The MVB interface 301 is provided with a male connector and a female connector, and has a rich external interface, so that the utility model has an MVB redundancy function and is suitable for a variety of application scenarios.** **[Page 11]** Among them, the host computer sends the data instructions received and sent by the test case during the test process. **The utility model receives the data instructions through TCP, decomposes the instruction parsing action through the embedded processor module, and then sends the data frame command to the FPGA module through the data bus and address bus and provides TTL level main frame data to the FPGA module.** The FPGA module sends the TTL level main frame data to the transceiver, and **the transceiver converts the received TTL level main frame data into RS485 level data and sends it to the MVB bus.** **The slave frame data replied by the MVB bus is converted into TTL level by the transceiver through the data buffer area. After the FPGA module collects the TTL level, it is sent to the embedded processor module for data processing and analysis.** **The embedded processor module feeds back the processed data to the host computer through TCP.**
Analyst Comments:	*This patent application broadly discloses*

*(**Note: X** – Represents that this reference when taken alone, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step; and Y - Represents that this reference can be relevant if combined with one or more references, such combination forms obviousness to a person skilled in the art)*	

Back to Analysis Summary

Publication No.	CN209514377U		
Title	A multifunction vehicle bus module		
Assignee/Applicant	Beijing Hollysys Co. Ltd.		
Earliest Priority Date	2019-04-30	Publication Date	2019-10-18

Abstract

The utility model discloses a multifunctional vehicle bus module. According to the module, a CPCI connector is arranged on the back of the module and is connected with an external power supply and a parallel bus; the field programmable gate array FPGA is connected with the CPCI connector; and the digital signal processor DSP is connected with the FPGA, a front panel of the module is a male-femaleDB9 connector, and the module is a standard module which is connected with the FPGA and has the size of 3U or 6U.

Description

[Page 4]

In an exemplary embodiment, the multi-function vehicle bus module further includes a multifunction vehicle bus (MVB) interface, referred to as MVB interface, and the MVB interface is located on the front panel of the multi-function vehicle bus module.

[Pages 11-12]

As shown in Figure 4, **the present application provides a standard 3U and 6U multi-function vehicle bus module implemented using FPGA and DSP,** which is powered by the baseboard CPCI connector; at the same time, the baseboard CPCI connector supports parallel bus, supporting parallel bus communication between the multi-function vehicle bus module and the main control CPU board through the baseboard. Among them, FPGA implements physical layer Manchester encoding and decoding functions specified in the IEC61375-1 protocol, and DSP implements link layer and above protocol functions. **The front panel has two DB9 MVB interfaces, one male and one female. In addition, the multifunctional vehicle bus module also includes two DPRAMs connected to the FPGA for communicating with the main control CPU board via a parallel bus. Based on the above structure, the multifunctional vehicle bus module can be conveniently installed inside the on-board automatic train protection equipment ATP (Automatic Train Protection, ATP) equipment cabinet.**

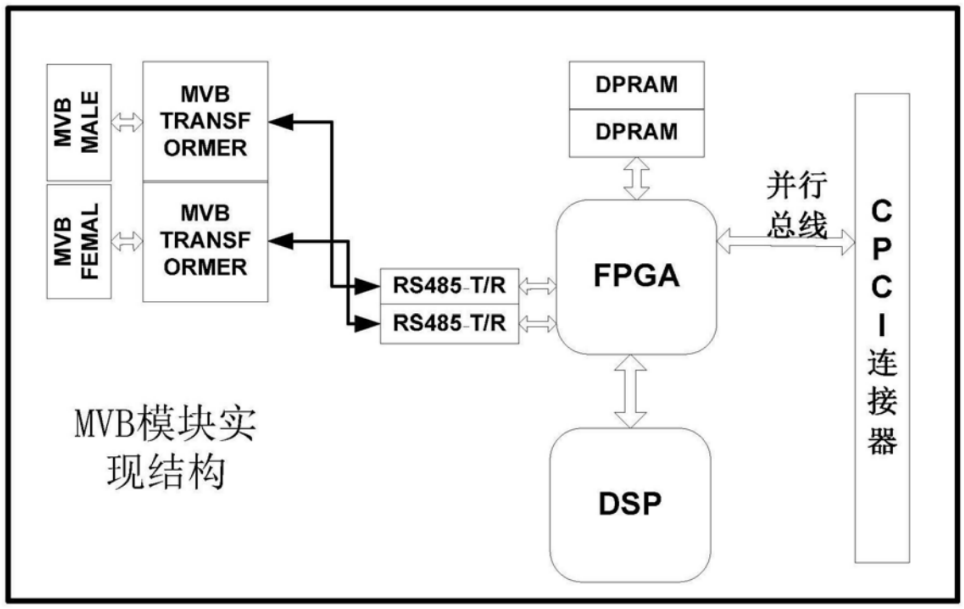


图4

Description

[Pages 11-12]

As shown in Figure 4, **the present application provides a standard 3U and 6U multi-function vehicle bus module implemented using FPGA and DSP,** which is powered by the baseboard CPCI connector; at the same time, the baseboard CPCI connector supports parallel bus, supporting parallel bus communication between the multi-function vehicle bus module and the main control CPU board through the baseboard. Among them, FPGA implements physical layer Manchester encoding and decoding functions specified in the IEC61375-1 protocol, and DSP implements link layer and above protocol functions. **The front panel has two DB9 MVB interfaces, one male and one female. In addition, the multifunctional vehicle bus module also includes two DPRAMs connected to the FPGA for communicating with the main control CPU board via a parallel bus. Based on the above structure, the multifunctional vehicle bus module can be conveniently installed inside the on-board automatic train protection equipment ATP (Automatic Train Protection, ATP) equipment cabinet.**

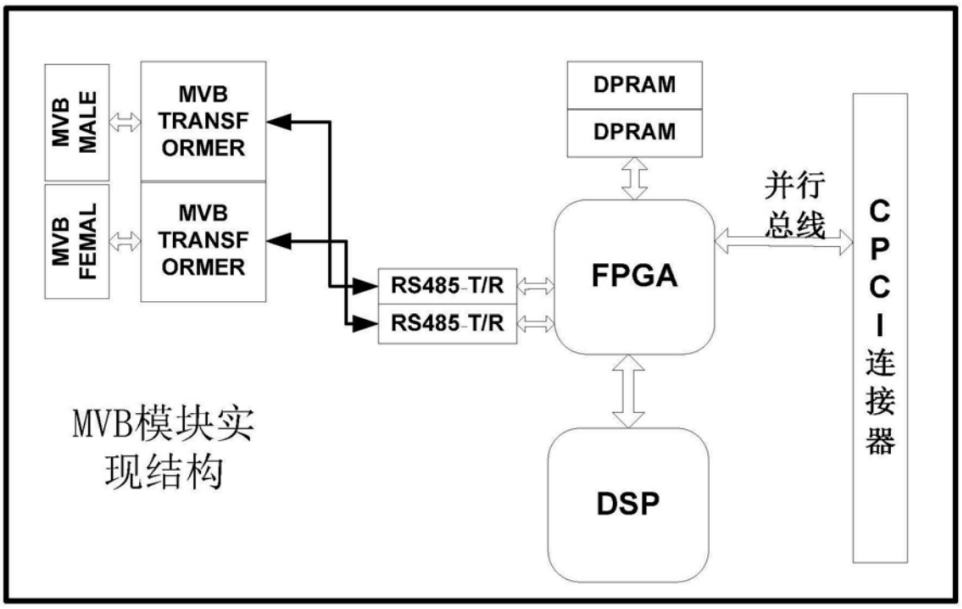


图4

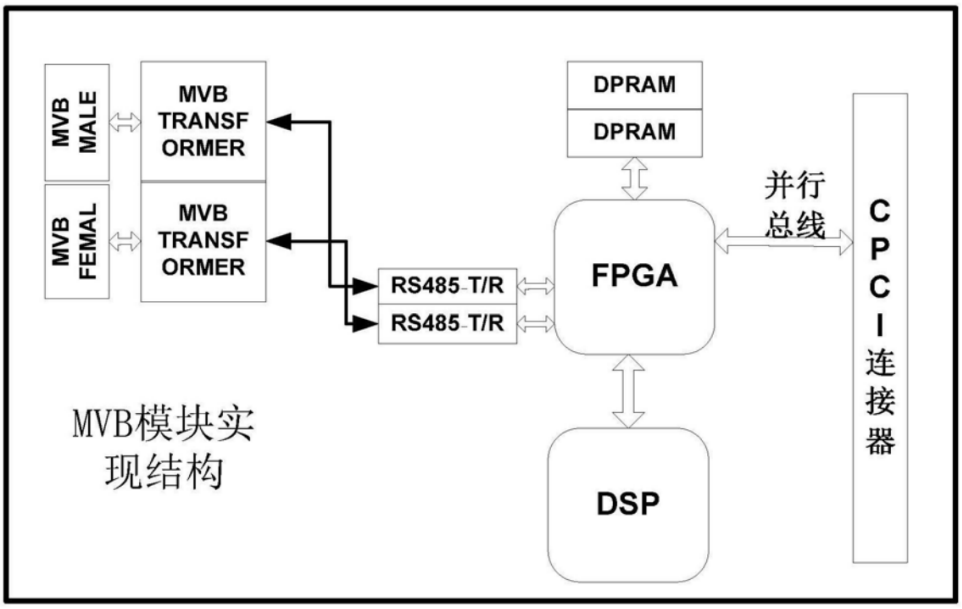
Description

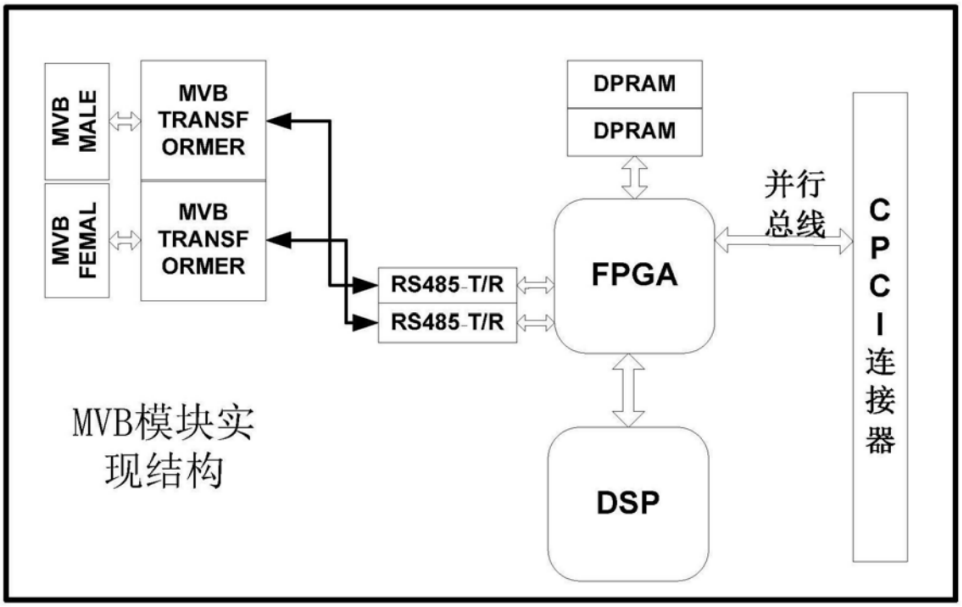
[Page 9]

In this exemplary embodiment, **the memory is connected to the FPGA via a parallel bus, so that the FPGA can read and write data using the memory in the multi-function vehicle bus module.**

In this exemplary embodiment, by setting the multifunctional vehicle bus module as a 3U or 6U standard module, it can be conveniently installed in a 3U cage or 6U cage of the vehiclemounted equipment. At the same time, with the help of the transmission characteristics of the parallel bus, **the purpose of data communication between the FPGA and the external main control CPU board is achieved. When the FPGA sends data to the main control CPU board, the FPGA reads the data from the memory and sends the data to the external main control CPU board through the CPCI connector; when the FPGA receives data from the main control CPU board, it receives the data from the main control CPU board through the CPCI connector and saves the received data to the memory.** Through the above data interaction, communication with the main control CPU motherboard can be completed to realize data transmission between units in the module.

[Pages 11-12]

	As shown in Figure 4, **the present application provides a standard 3U and 6U multi-function vehicle bus module implemented using FPGA and DSP,** which is powered by the baseboard CPCI connector; at the same time, the baseboard CPCI connector supports parallel bus, supporting parallel bus communication between the multi-function vehicle bus module and the main control CPU board through the baseboard. Among them, FPGA implements physical layer Manchester encoding and decoding functions specified in the IEC61375-1 protocol, and DSP implements link layer and above protocol functions. **The front panel has two DB9 MVB interfaces, one male and one female. In addition, the multifunctional vehicle bus module also includes two DPRAMs connected to the FPGA for communicating with the main control CPU board via a parallel bus. Based on the above structure, the multifunctional vehicle bus module can be conveniently installed inside the on-board automatic train protection equipment ATP (Automatic Train Protection, ATP) equipment cabinet.**  图4
	Description **[Page 6]** **A digital signal processor DSP is connected to the FPGA.** **[Page 7]** In this exemplary embodiment, the FPGA implements functions mainly to encode and parse data on the physical layer, and send the parsed data to the link layer module to parse

	the protocol. The MVB protocol communication rate is fixed at 1.5Mbps. Its frame format is divided into two types: master frame and slave frame. Manchester encoding is used for encoding and decoding operations. FIG. 2 is a schematic diagram of an encoding method specified in the IEC 61375-1 protocol provided in an embodiment of the present application. **In an exemplary embodiment, the DSP is a module for implementing protocol functions of the link layer and layers above it.**  图4
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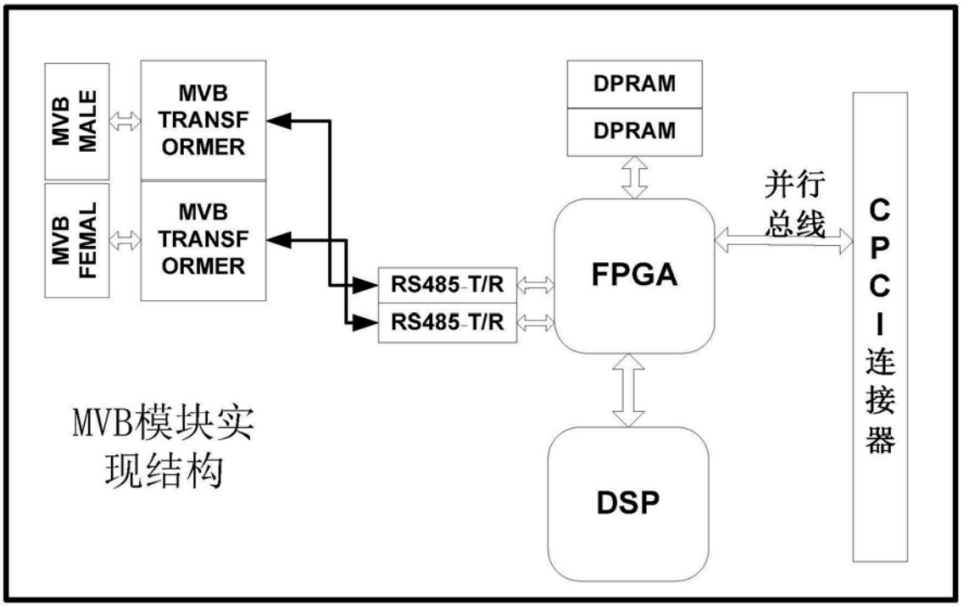
	Description **[Page 6]** **Compact Peripheral Component Interconnect (CPCI) connector, which connects the external power supply and the parallel bus;** **[Pages 11-12]** As shown in Figure 4, **the present application provides a standard 3U and 6U multi-function vehicle bus module implemented using FPGA and DSP, which is powered by the baseboard CPCI connector; at the same time, the baseboard CPCI connector supports parallel bus, supporting parallel bus communication between the multi-function vehicle bus module and the main control CPU board through the baseboard.** Among them, FPGA implements physical layer Manchester encoding and decoding functions specified in the IEC61375-1 protocol, and DSP implements link layer

	and above protocol functions. The front panel has two DB9 MVB interfaces, one male and one female. In addition, the multifunctional vehicle bus module also includes two DPRAMs connected to the FPGA for communicating with the main control CPU board via a parallel bus. Based on the above structure, the multifunctional vehicle bus module can be conveniently installed inside the on-board automatic train protection equipment ATP (Automatic Train Protection, ATP) equipment cabinet.  图4
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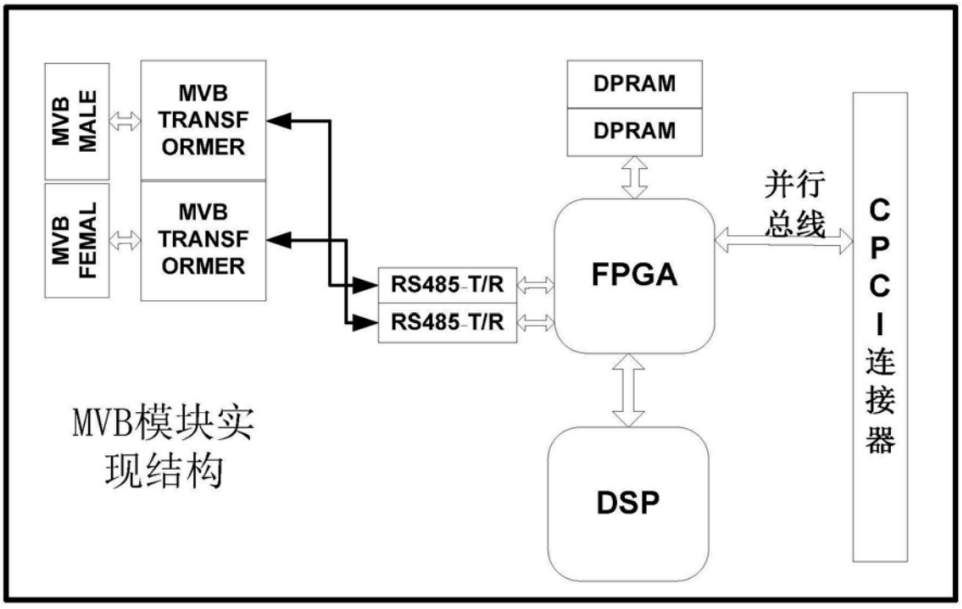
	Description **[Page 12]** The module provided in the embodiment of the present application adopts DSP instead of ARM. DSP is widely used in the industrial field, and the chip life cycle is more than several decades, which matches the train use cycle. **In addition, the module interface adopts the baseboard parallel bus mode, and the module size is designed as a standard module of 3U or 6U, which can be easily installed in the vehicle's existing on-board equipment cage, and at the same time supports the main control CPU**

	module to be accessed through the baseboard parallel bus, with good real-time performance. **[Pages 11-12]** As shown in Figure 4, **the present application provides a standard 3U and 6U multi-function vehicle bus module implemented using FPGA and DSP, which is powered by the baseboard CPCI connector; at the same time, the baseboard CPCI connector supports parallel bus, supporting parallel bus communication between the multi-function vehicle bus module and the main control CPU board through the baseboard.** Among them, FPGA implements physical layer Manchester encoding and decoding functions specified in the IEC61375-1 protocol, and DSP implements link layer and above protocol functions. The front panel has two DB9 MVB interfaces, one male and one female. In addition, the multifunctional vehicle bus module also includes two DPRAMs connected to the FPGA for communicating with the main control CPU board via a parallel bus. Based on the above structure, the multifunctional vehicle bus module can be conveniently installed inside the on-board automatic train protection equipment ATP (Automatic Train Protection, ATP) equipment cabinet.  图4
	Description **[Page 10]**

In this exemplary embodiment, by setting the multifunctional vehicle bus module as a 3U or 6U standard module, it can be conveniently installed in a 3U cage or 6U cage of the vehicle mounted equipment. At the same time, with the help of the transmission characteristics of the parallel bus, the purpose of data communication between the FPGA and the external main control CPU board is achieved. When the FPGA sends data to the main control CPU board, the FPGA reads the data from the memory and sends the data to the external main control CPU board through the CPCI connector; when the FPGA receives data from the main control CPU board, it receives the data from the main control CPU board through the CPCI connector and saves the received data to the memory. Through the above data interaction, communication with the main control CPU motherboard can be completed to realize data transmission between units in the module.

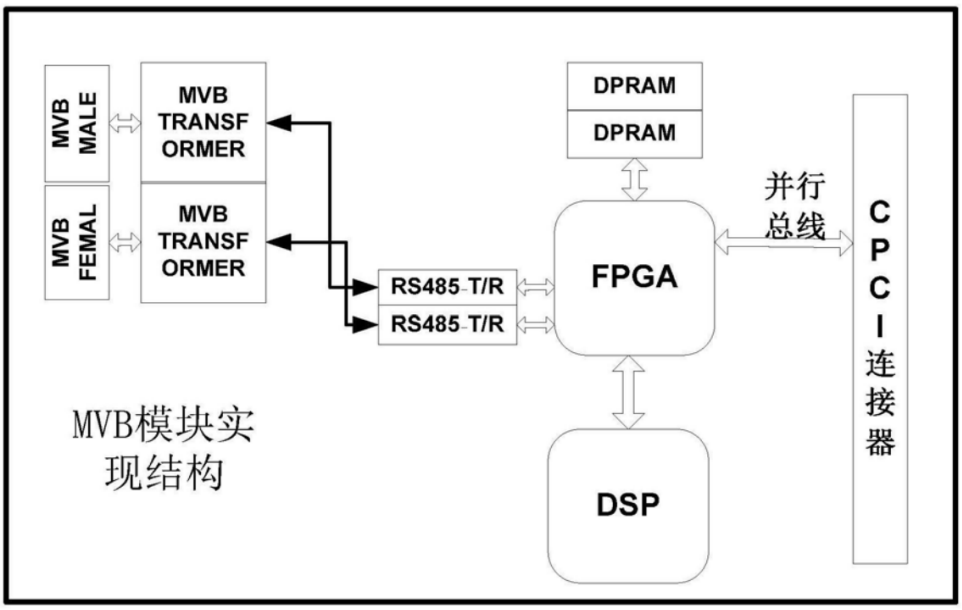
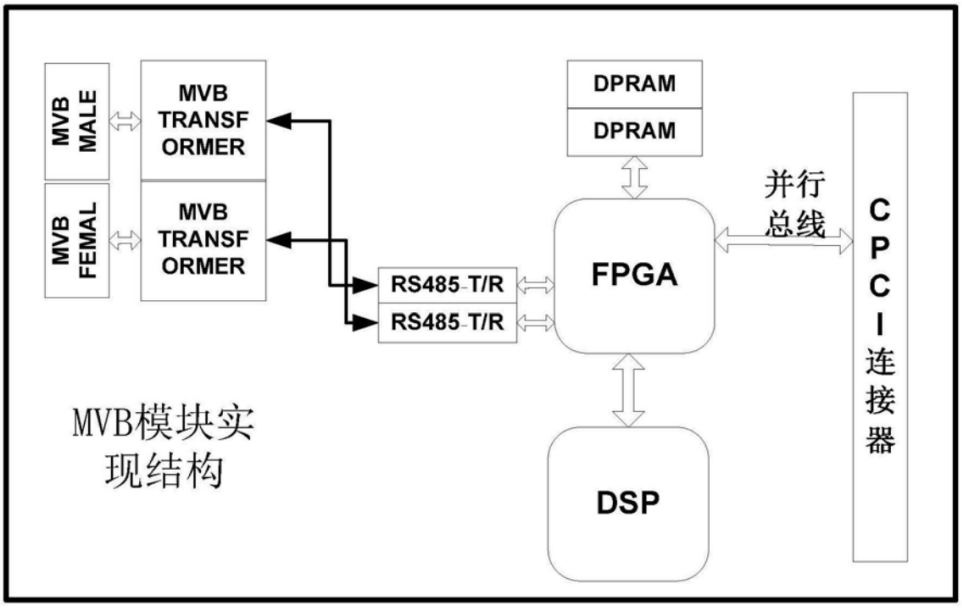


图4

[Page 12]

The multifunctional vehicle bus module provided in the embodiment of the present application utilizes DSP instead of ARM to realize corresponding functions, thereby ensuring that the replacement cycle of the multifunctional vehicle bus module matches the use cycle in the train; **by designing the module size to 3U or 6U, it is installed in the 3U cage or 6U cage of the on-board equipment, and utilizing a parallel bus to realize communication between the multifunctional vehicle bus module and the main control CPU board.**

	Description **[Page 12]** The module provided in the embodiment of the present application adopts DSP instead of ARM. DSP is widely used in the industrial field, and the chip life cycle is more than several decades, which matches the train use cycle. **In addition, the module interface adopts the baseboard parallel bus mode, and the module size is designed as a standard module of 3U or 6U, which can be easily installed in the vehicle's existing on-board equipment cage, and at the same time supports the main control CPU module to be accessed through the baseboard parallel bus, with good real-time performance.**
	Description **[Page 9]** In this exemplary embodiment, by setting the multifunctional vehicle bus module as a 3U or 6U standard module, it can be conveniently installed in a 3U cage or 6U cage of the vehicle mounted equipment. At the same time, **with the help of the transmission characteristics of the parallel bus, the purpose of data communication between the FPGA and the external main control CPU board is achieved. When the FPGA sends data to the main control CPU board, the FPGA reads the data from the memory and sends the data to the external main control CPU board through the CPCI connector; when the FPGA receives data from the main control CPU board, it receives the data from the main control CPU board through the CPCI connector and saves the received data to the memory. Through the above data interaction, communication with the main control CPU motherboard can be completed to realize data transmission between units in the module.** **[Page 11]** In this exemplary embodiment, **the first RS485 chip, the male DB9 type MVB interface and the FPGA form one data transmission channel, and the second RS485 chip, the female DB9 type MVB interface and the FPGA form another data transmission channel.** **[Pages 11-12]** As shown in Figure 4, the present application provides a standard 3U and 6U multi-function vehicle bus module implemented using FPGA and DSP, which is powered by the baseboard CPCI connector; at the same time, the baseboard CPCI connector supports parallel bus, supporting parallel bus communication between the multi-function vehicle

	bus module and the main control CPU board through the baseboard. Among them, **FPGA implements physical layer Manchester encoding and decoding functions specified in the IEC61375-1 protocol, and DSP implements link layer and above protocol functions. The front panel has two DB9 MVB interfaces, one male and one female.** In addition, the multifunctional vehicle bus module also includes two DPRAMs connected to the FPGA for communicating with the main control CPU board via a parallel bus. Based on the above structure, the multifunctional vehicle bus module can be conveniently installed inside the on-board automatic train protection equipment ATP (Automatic Train Protection, ATP) equipment cabinet.  图4
Analyst Comments: *(**Note: X** – Represents that this reference when taken alone, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step; and Y - Represents that this reference can be*	*This patent application broadly discloses an*

relevant if combined with one or more references, such combination forms obviousness to a person skilled in the art)	

Back to Analysis Summary

Publication No.	US9565270B2		
Title	LPC2468-based MVB-WTB gateway and working method thereof		
Assignee/Applicant	Institute of Software of CAS		
Earliest Priority Date	2012-10-11	Publication Date	2017-02-07

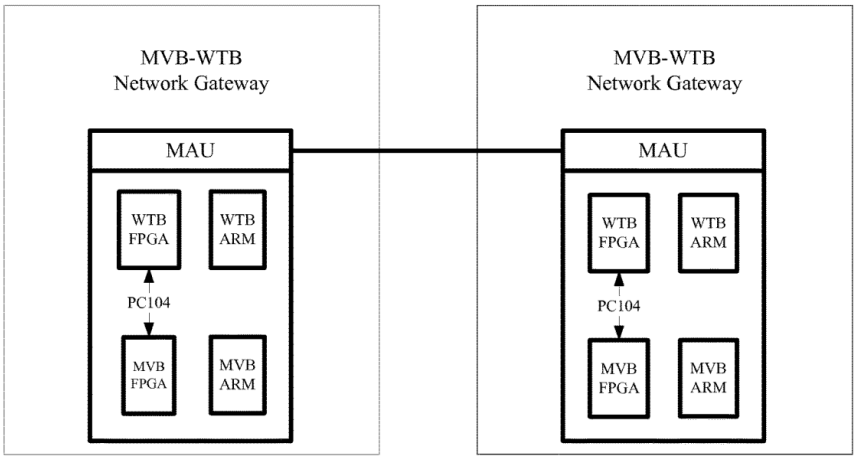
Abstract

The present invention discloses a LPC2468-based MVB-WTB gateway and associated operating methods in the field of train communications. The disclosed network gateway includes a MVB network card and a WTB network card. The WTB network card includes WTB-ARM and a WTB-FPGA module. The MVB network card includes MVB-ARM and MVB-FPGA module. The WTB-ARM module uses a LPC2468 processor to analyze data in the network layer and the data link layer based on gateway protocol. The WTB-FPGA module allows WTB to exchange data with other networks gateways, as well as between the WTB and MVB. The MVB-ARM module is responsible for executing protocols on the network cards. Via data communications on MVB, the MVB-FPGA module collects the process and message data of the MVB equipment, and exchange communication data between WTB within a network gateway. The present invention can increase speed and enhance reliability for communications between gateways.

Description

[Page 5, Col. 3, Lines 43-64]

In terms of hardware, **a LPC2468-based MVB-WTB Gateway includes: a WTB-ARM module, a WTB-FPGA module, an MVB-ARM module, an MVB-FPGA module, an MAU board, a PC104 bus, an MVB interface, an MAU interface**, a WTB serial interface, an MVB serial interface, an MVB manual reset button, a WTB manual reset button, and a power supply interface. An MVB network card equipped with a PC104 interface collects process and message data about MVB equipment transmitted over the main data bus. The MVB network card is connected to a WTB network card via a PC104 bus; and the process and message data is transmitted from the MVB network card to the WTB network card. A MAU card that is connected to the WTB network card is a media connecting unit. The MAU card is part of the network gateway and is electrically connected to the main data bus. The MAU card provides and receives binary logic signals; forwards data received from the main data bus; and transmits data from the MVB network card via the WM network card. By connecting MAU cards in two MVB-WTB gateways, communications between

	the two network gateways are established, and data interoperability between the two network segments is achieved.  **Figure 1**
	Description **[Page 5, Col. 3, Lines 43-64]** In terms of hardware, **a LPC2468-based MVB-WTB Gateway includes: a WTB-ARM module, a WTB-FPGA module, an MVB-ARM module, an MVB-FPGA module, an MAU board, a PC104 bus, an MVB interface, an MAU interface**, a WTB serial interface, an MVB serial interface, an MVB manual reset button, a WTB manual reset button, and a power supply interface. An MVB network card equipped with a PC104 interface collects process and message data about MVB equipment transmitted over the main data bus. The MVB network card is connected to a WTB network card via a PC104 bus; and the process and message data is transmitted from the MVB network card to the WTB network card. A MAU card that is connected to the WTB network card is a media connecting unit. The MAU card is part of the network gateway and is electrically connected to the main data bus. The MAU card provides and receives binary logic signals; forwards data received from the main data bus; and transmits data from the MVB network card via the WM network card. By connecting MAU cards in two MVB-WTB gateways, communications between the two network gateways are established, and data interoperability between the two network segments is achieved.

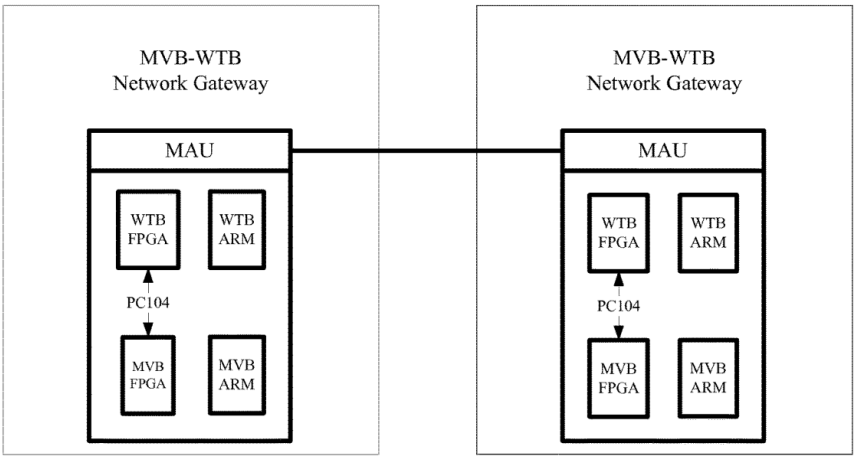
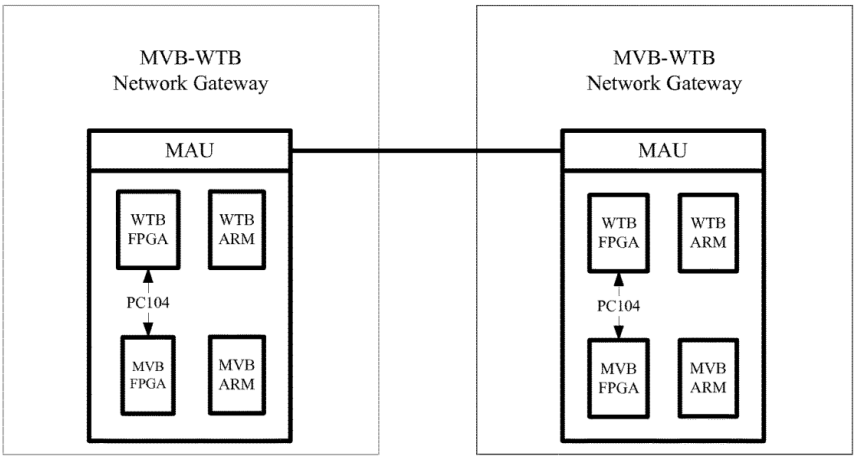


Figure 1

Description

[Page 5, Col. 3, Lines 43-64]

In terms of hardware, **a LPC2468-based MVB-WTB Gateway includes: a WTB-ARM module, a WTB-FPGA module, an MVB-ARM module, an MVB-FPGA module, an MAU board, a PC104 bus, an MVB interface, an MAU interface**, a WTB serial interface, an MVB serial interface, an MVB manual reset button, a WTB manual reset button, and a power supply interface. An MVB network card equipped with a PC104 interface collects process and message data about MVB equipment transmitted over the main data bus. The MVB network card is connected to a WTB network card via a PC104 bus; and the process and message data is transmitted from the MVB network card to the WTB network card. A MAU card that is connected to the WTB network card is a media connecting unit. The MAU card is part of the network gateway and is electrically connected to the main data bus. The MAU card provides and receives binary logic signals; forwards data received from the main data bus; and transmits data from the MVB network card via the WM network card. By connecting MAU cards in two MVB-WTB gateways, communications between the two network gateways are established, and data interoperability between the two network segments is achieved.

	 **Figure 1** **[Page 5, Col. 4, Lines 5-10]** **2) The WTB-FPGA modules: its function includes, first, transmitting and receiving communication data between the WTB network card of the same gateway with other network gateways, and secondly, exchanging communication data between the WTB and the MVB network card within the present gateway.** **[Page 5, Col. 4, Lines 39-45]** **A: A WTB FPGA chip board comprising a LPC2468 based hard core is integrated with an MVB board. FPGA is used for communications, which make communications more stable. In the communication process between WTB and WTB, the fast-response characteristics in FPGA allows increased communication speeds between network gateways, which enhances reliability.**
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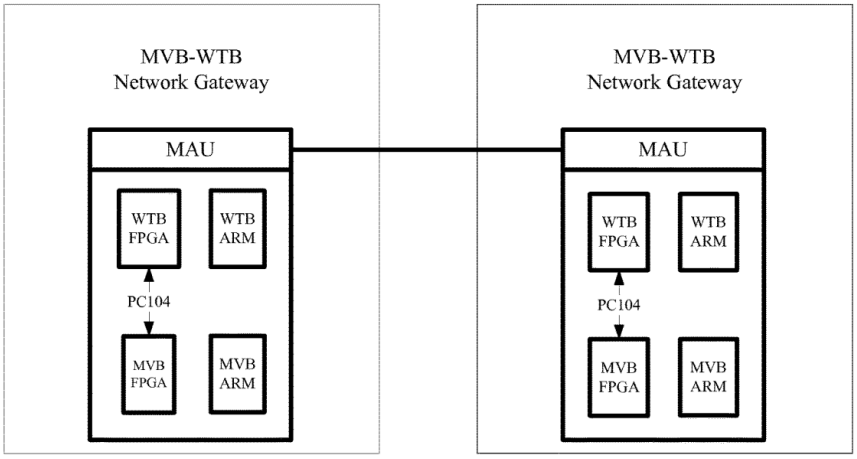
	-
	Summary **[Page 4, Col. 2, Lines 41-57]** The main data bus is implemented by a PC104 bus, wherein the MVB network card is connected with the WTB network card via the PC104 bus, wherein each gateway further includes a MAU card configured to communicate with other network gateways, wherein the MAU card is connected to the WTB main bus, wherein each gateway further includes a WTB serial interface and a MVB serial interface, wherein

	the MVB serial interface is configured to provide maintenance and debugging for the MVB network card, wherein the WTB serial interface is configured to provide maintenance and debugging for the WTB network card, wherein the MVB network card also includes a manual reset key to be used for MVB reset operation, wherein the WTB network card includes a WTB manual reset button to be used for WTB reset operation, **the LPC2468-based MVB-WTB network gateway further comprising a power interface configured to supply power.**  **Figure 1** **[Page 5, Col. 4, Lines 34-35]** **13) The power Interface: it is used to supply power to MVB-WTB gateway devices**
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	-
	-
	-
	Technical Field **[Page 4, Col. 1, Lines 6-11]** **The present invention relates to the field of train communications, and in particular to LPC2468-based MVB-WTB gateway and its working method.**

	Gateway is the most important part of train communications; its real-time performance, stability, and reliability play a vital role in the trains' safe operations. **Summary** **[Page 4, Col. 2, Lines 37-40]** **The WTB-FPGA module can periodically poll the main frame table at each MVB-WTB gateway node, wherein the WTB-FPGA module can sporadically send monitoring data to the main data bus.**
	Summary **[Page 4, Col. 2, Lines 1-20]** An LPC2468-based MVB-WTB network gateway includes an MVB network card comprising: an MVB-ARM module; and an MVB-FPGA module; and a WTB network card comprising: WTB-ARM module; and a WTB-FPGA module, **wherein the WTB network card and the MVB network card are connected by a main data bus, wherein the WTB-ARM module includes a LPC2468 based processor configured to analyze data in the network layer and the data link layer in gateway protocol, wherein the WTB-FPGA module is configured to send data to and receive data from other network gateways, and to exchange communication data between the WTB network card and the MVB network card in the same network gateway, wherein the MVB-ARM module is configured to execute a protocol stack in the MVB network card, wherein the MVB-FPGA module is configured to collect process and message data about MVB equipment, and exchange communication data between the WTB network card and the MVB network card within the network gateway.** **Description** **[Page 5, Col. 4, Lines 5-10]** **2) The WTB-FPGA modules: its function includes, first, transmitting and receiving communication data between the WTB network card of the same gateway with other network gateways, and secondly, exchanging communication data between the WTB and the MVB network card within the present gateway.**
Analyst Comments:	*This patent application broadly discloses*

*(**Note: X** – Represents that this reference when taken alone, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step; and Y - Represents that this reference can be relevant if combined with one or more references, such combination forms obviousness to a person skilled in the art)*	

9. List of Additional Patents and Non-Patent Literature

Back to Analysis Summary

Related Published Patents and Non-Patent Literatures found during this search, which may be of relevance for the client				
S. No.	**Publication/Patent Number**	**Title**	**Assignee**	**Filing Date**
1	US9669732B2	Traction control system for electric multiple units	Crrc Qingdao Sifang Rolling Stock Research Institute Co. Ltd.	2015-05-20
2	CN205210536U	Digital output module of redundant output based on special cpu	China Electronics Corp.	2015-12-14
3	CN118465390A	Vehicle-mounted atc system host cabinet testing device	Beijing Railway Signal Co Ltd	2023-02-09
4	RU178759U1	Testing mobile device for can network configuration	Limited Liability Company Marathon	2017-12-28
5	CN101123592B	Mvb-can gateway based on arm7 micro processor	China Cnr Corp Ltd Dalian Elec	2007-05-24
6	CN103279109B	Locomotive digital value collecting device based on mvb bus	Crrc Zhuzhou Institute Co. Ltd.	2013-06-09
7	CN100534273C	Locomotive/vehicle control module structure	Zhuzhou CRRC Times Electric Co Ltd	2006-06-26
8	NPL 1	PCI Express Mini Card MVB Interface	Duagon	-
9	NPL 2	MVB Interface	Duagon	-

10. Exemplary Search Strings

Back to Analysis Summary

S. No.	Scope	Query	No. of hits
1	Patent literature	(ttl_en:(("mvb" OR (multifunction NEAR2 vehicle NEAR3 bus))) AND ((rail OR railcar OR railcars OR railway OR locomotive OR locomotives) OR (train OR trains)) AND ("FPGA" OR "Field Programmable Gate Array" OR "field-programmable gate array") AND (enclosure OR enclosures OR box OR boxes OR container OR containers OR case OR cases OR shell OR shells))	35
2		(ab_en:(("mvb" OR (multifunction NEAR2 vehicle NEAR3 bus)) NEAR2 (module OR modules)) AND desc_en:((rail OR railcar OR railcars OR railway) OR (train OR trains)) AND desc_en:("FPGA" OR "Field Programmable Gate Array" OR "field-programmable gate array"))	29
3		(tac_en:(("mvb" OR (multifunction NEAR2 vehicle NEAR3 bus)) NEAR2 (module OR modules OR interface OR interfaces)) AND desc_en:((rail OR railcar OR railcars OR railway) OR (train OR trains)) AND desc_en:("FPGA" OR "Field Programmable Gate Array" OR "field-programmable gate array") AND desc_en:((data OR compliance) NEAR2 (communication OR communicate OR (transmitting OR transmit OR transmitted OR transmitability) OR (transfer OR transfers OR transferable OR transference OR transferability OR transferer))))	3
4		(tac_en:(("mvb" OR (multifunction NEAR2 vehicle NEAR3 bus)) NEAR3 (module OR modules OR interface OR interfaces)) AND desc_en:((rail OR railcar OR railcars OR railway) OR (train OR trains)) AND desc_en:("FPGA" OR "Field Programmable Gate Array" OR "field-programmable gate array") AND desc_en:(signal OR signalling OR signaling OR signals OR filters OR filter) AND desc_en:(networks))	32
5		(tac_en:("mvb" OR (multifunction NEAR2 vehicle NEAR3 bus)) AND desc_en:((rail OR railcar OR railcars OR railway) OR (train OR trains)) AND desc_en:("FPGA" OR "Field Programmable Gate Array" OR "field-programmable gate array") AND desc_en:(signal OR signalling OR signaling OR signals OR filters OR filter))	263
6		(clm_en:(("mvb" OR (multifunction NEAR2 vehicle NEAR3 bus))) AND desc_en:((rail OR railcar OR railcars OR railway) OR (train OR trains)) AND desc_en:("FPGA" OR "Field Programmable Gate Array" OR "field-programmable gate array") AND desc_en:(enclosure OR enclosures OR box OR boxes OR container OR containers))	36
7		(desc_en:(("mvb" OR (multifunction NEAR2 vehicle NEAR3 bus))) AND desc_en:((rail OR railcar OR railcars OR railway) OR (train OR trains) OR (locomotives)) AND desc_en:("FPGA" OR "Field Programmable Gate Array" OR "field-programmable gate array") AND desc_en:((enclosed OR enclose OR enclosing OR enclosure OR enclosures) OR enclosures OR (boxes OR boxing OR boxed OR boxful) OR boxes OR container OR containers OR (case OR casings OR cased OR caseful) OR cases) AND desc_en:(vibration OR vibrating OR (rugged OR ruggedly OR ruggedisation OR ruggedised OR ruggedization OR ruggedize OR ruggedness OR ruggedized) OR shake OR shaking OR (shaking OR shakes) OR (harsh OR harshness OR harshly)) AND desc_en:("emi" OR "emf" OR (magnetic OR magnets OR	18

		magnetically OR magnetism OR magnetization OR magnetize OR magnetics) OR "emc" OR (electromagnetic OR electromagnet OR electromagnetism)))	
8		(("MVB" OR "MVB Communication Module ") AND ("FPGA").ti.)	4
9		(("MVB" OR "MVB Communication Module ") AND ("FPGA").ti. ab.)	20
10		((((("mvb" OR (multifunction NEAR2 vehicle NEAR3 bus)) NEAR2 (module OR modules OR interface OR interfaces OR device OR devices)) AND ((rail OR railcar OR railcars OR railway) OR (train OR trains)) AND ("FPGA" OR "Field Programmable Gate Array" OR "field-programmable gate array") AND (enclosure OR enclosures OR box OR boxes OR container OR containers))clm.)	4
11		(("mvb" OR (multifunction NEAR2 vehicle NEAR3 bus)) NEAR2 (module OR modules)) AND ((rail OR railcar OR railcars OR railway) OR (train OR trains)) AND ("FPGA" OR "Field Programmable Gate Array" OR "field-programmable gate array").clms.	2
12		(("mvb" OR (multifunction NEAR2 vehicle NEAR3 bus)) NEAR2 (module OR modules OR interface OR interfaces OR device OR devices)) AND (enclosure OR enclosures OR box OR boxes OR container OR containers).detd.	16
13		(H04L12/40.cpc.) and (("mvb" OR (multifunction adj vehicle adj bus)) and (module OR modules OR interface OR interfaces OR device OR devices))clm.	26
14		(("mvb" OR (multifunction adj vehicle adj bus)) and ((enclosed OR enclose OR enclosing OR enclosure OR enclosures) OR (boxes OR boxing OR boxed OR boxful) OR container OR containers OR (case OR casings OR cased OR caseful) OR cases) AND (vibration OR vibrating OR (rugged OR ruggedly OR ruggedisation OR ruggedised OR ruggedization OR ruggedize OR ruggedness OR ruggedized) OR shake OR (shaking OR shakes) OR (harsh OR harshness OR harshly)))detd.	231
15		(("mvb" OR (multifunction NEAR2 vehicle NEAR3 bus))) AND ((rail OR railcar OR railcars OR railway) OR (train OR trains)) AND ("FPGA" OR "Field Programmable Gate Array" OR "field-programmable gate array").detd	375
16		(H04L12/40.cpc.) AND (("mvb" OR (multifunction adj vehicle adj bus)).ti. and (rugged OR ruggedly OR ruggedisation OR ruggedised OR ruggedization OR ruggedize OR ruggedness OR ruggedized) OR shake OR (shaking OR shakes) OR (harsh OR harshness OR harshly))detd.	100
17		(Beijing Hollysys.as. AND (China Academy of Railway Sciences).as. AND (Zhengzhou Railway).as.) AND ("MVB").detd. AND ("fpga").detd.	114
18		("MVB module" OR "Multifunction Vehicle Bus") AND (FPGA OR "Field Programmable Gate Array") AND ("real-time communication" OR "deterministic communication")	33
19		"mvb" "module" "fpga" "shock"	12
20	Non-Patent literature	"mvb" "communication module" with case enclosure fpga rugged	80
21		"mvb" "fpga" "harsh environment" "enclosure" "case"	40
22		“Multifunction vehicle bus” "communication module" rolling stocks	47
23		"mvb communication module" with “fpga”	4
24		enclosed “mvb” module for railways	100

Data Availability:

- ✓ Documents from non-English countries was restricted to the availability of the text in free and commercial databases (most of the cases only Title and Abstract are available in English)
- ✓ Search was performed with English keywords and their synonyms. Any language other than English such as French, Korean, and Chinese was not considered for the key string.

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